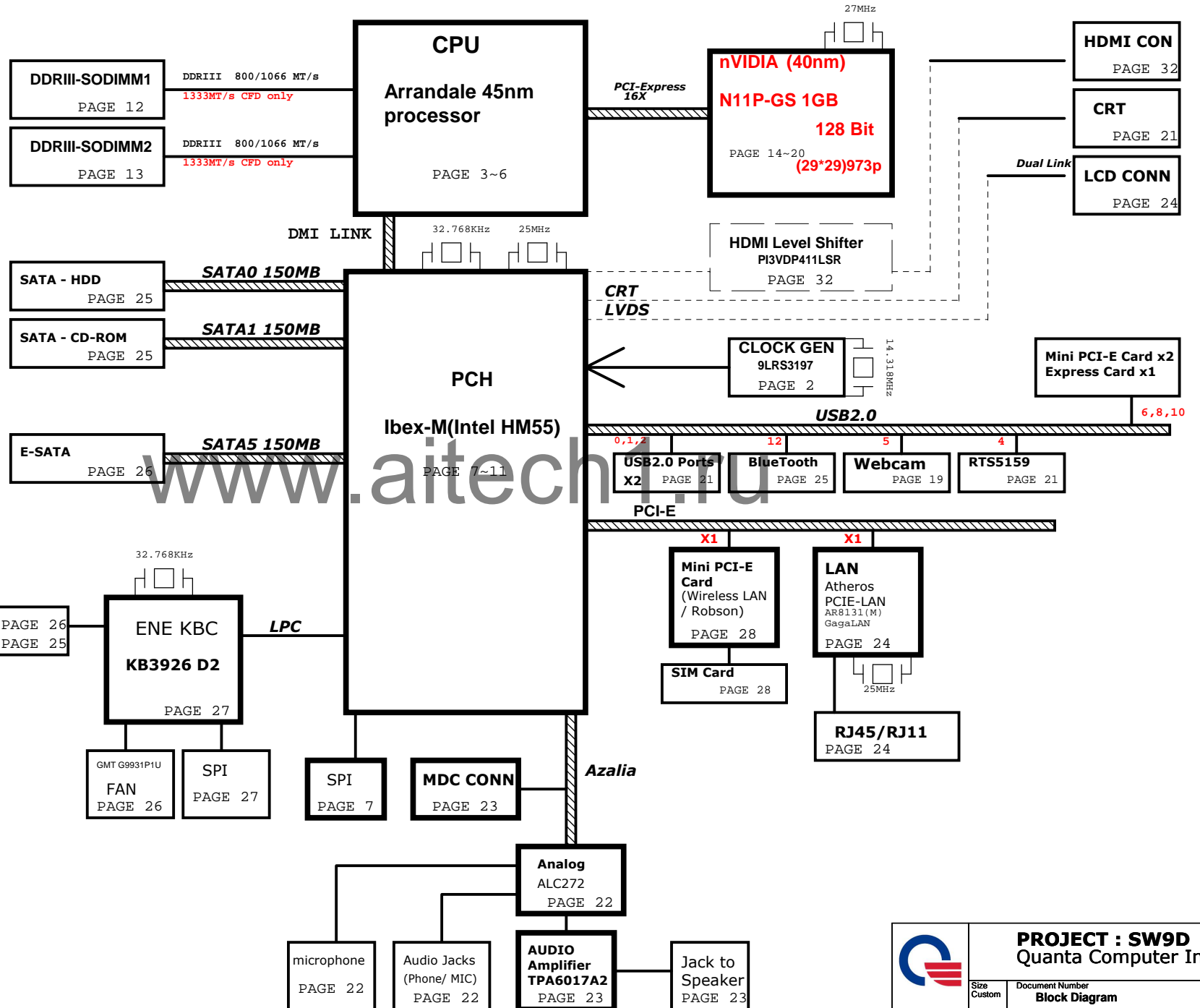
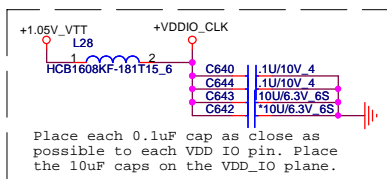


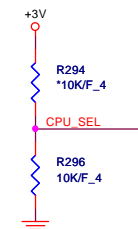
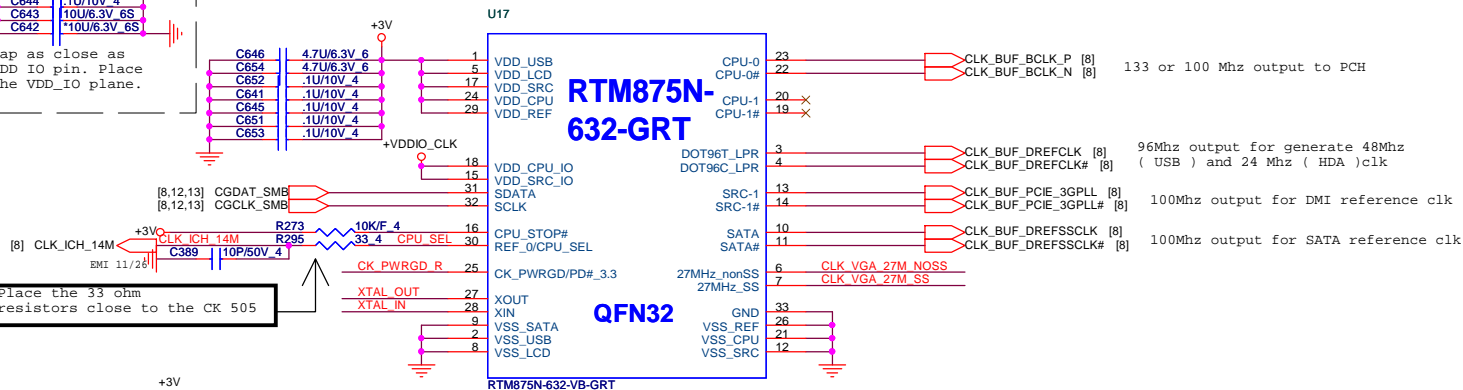
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(high)
LAYER 4 : IN2(low)
LAYER 5 : VCC
LAYER 6 : IN3(high)
LAYER 7 : GND
LAYER 8 : BOT



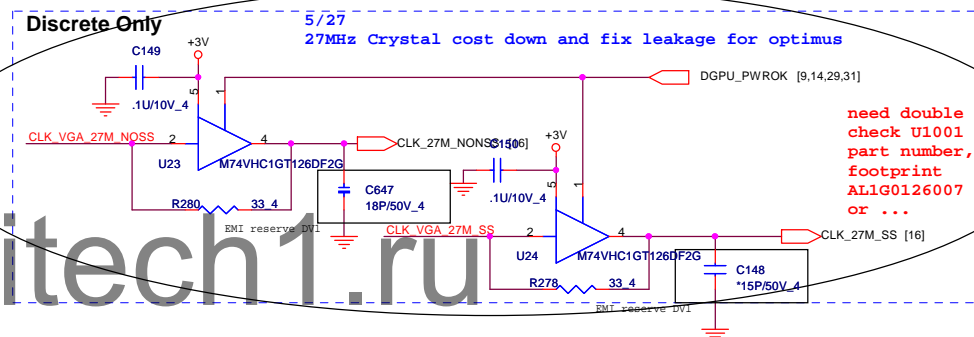
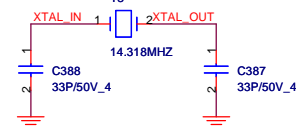
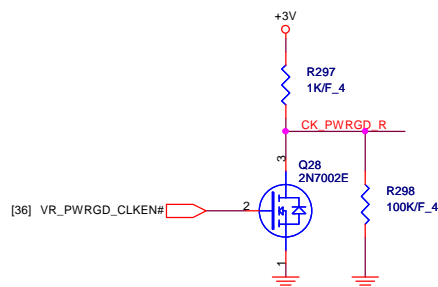
CLOCK GENERATOR



Place each 0.1uF cap as close as possible to each VDD IO pin. Place the 10uF caps on the VDD IO plane.



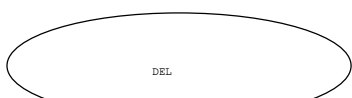
	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz



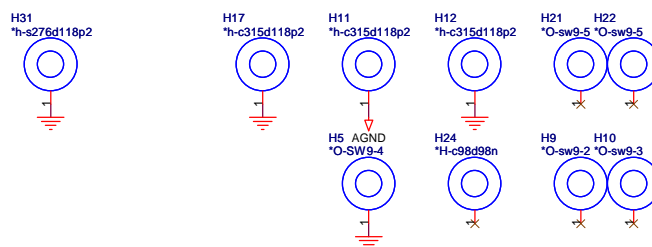
need double
check U1001
part number,
footprint
AL1G0126007
or ...

www.aitech1.ru

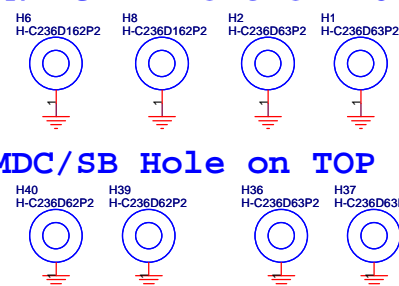
CPU bracket Hole.



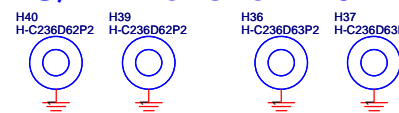
PAD and HOLE



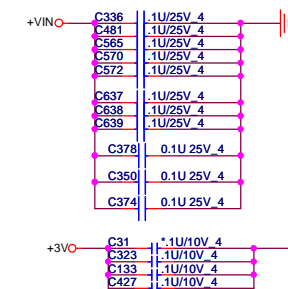
MINI CARD Hole on BOT Side



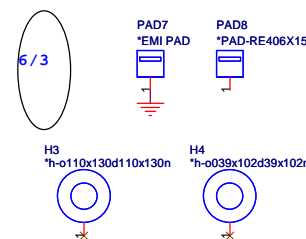
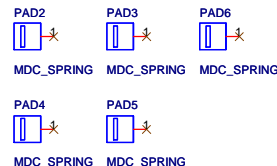
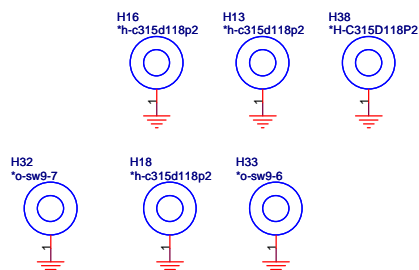
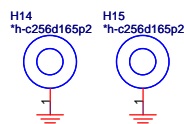
MDC/SB Hole on TOP Side



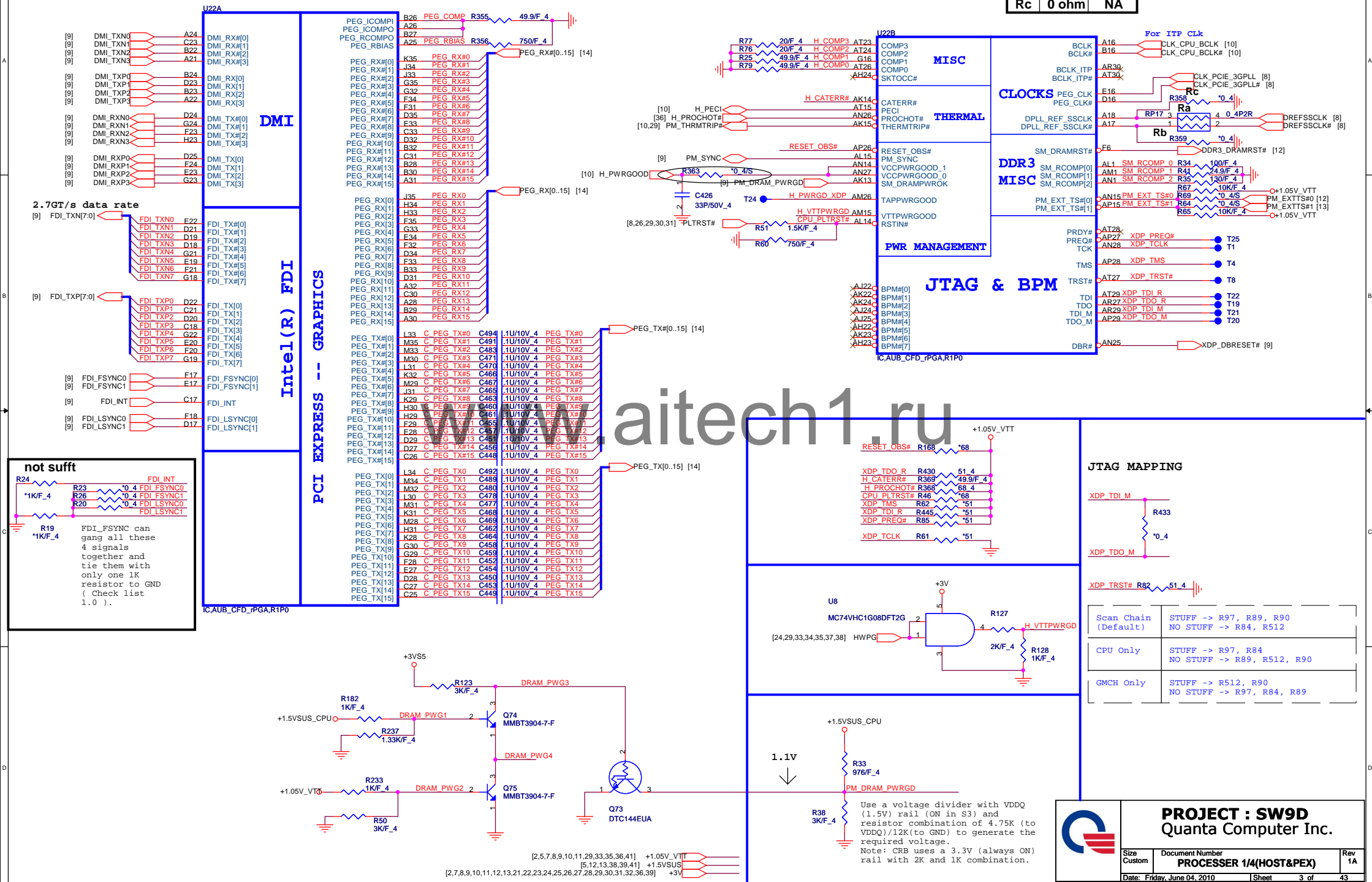
EMI capacitive



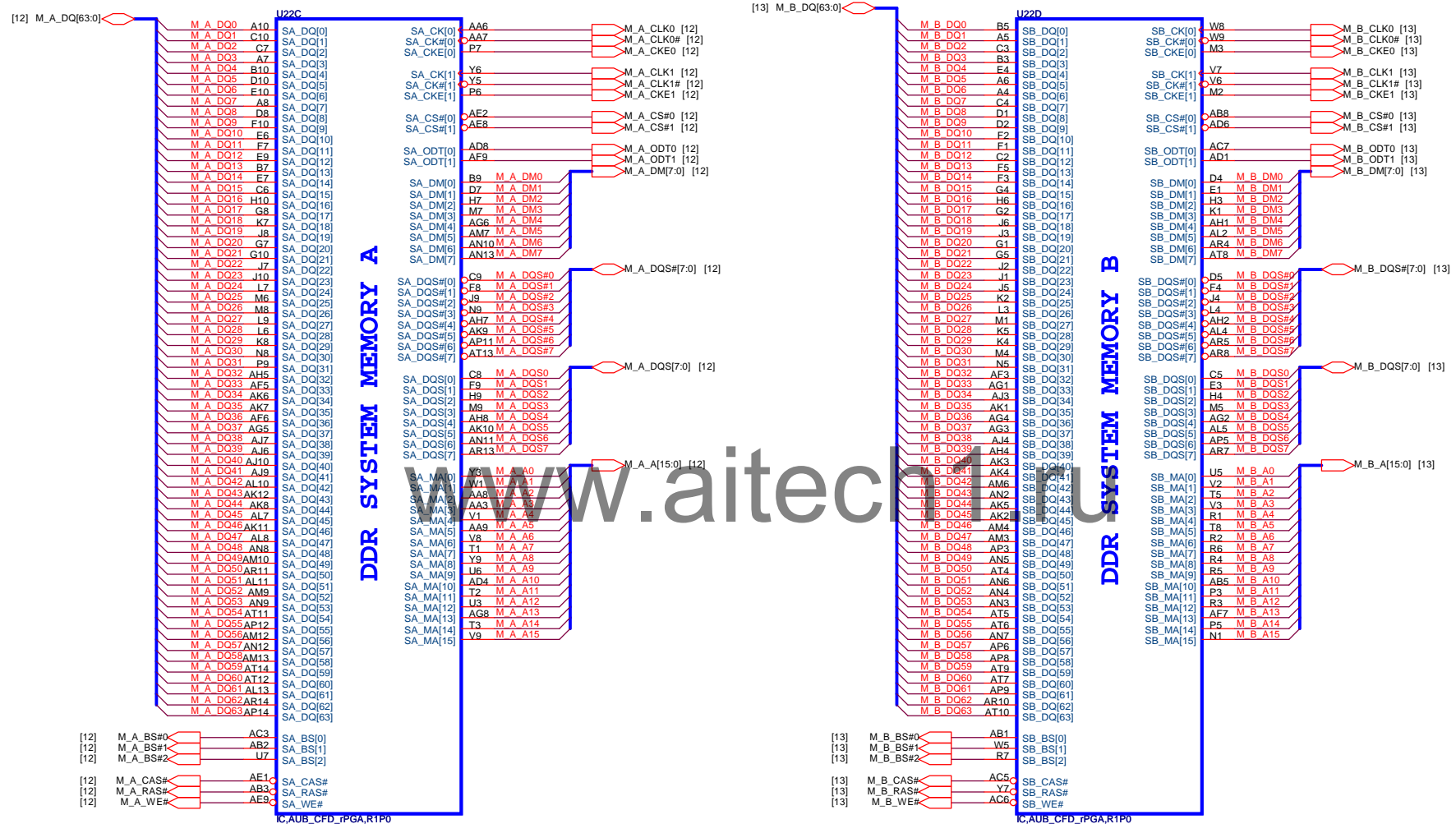
VGA bracket Hole.



	DIS	UMA
Ra	0 NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA



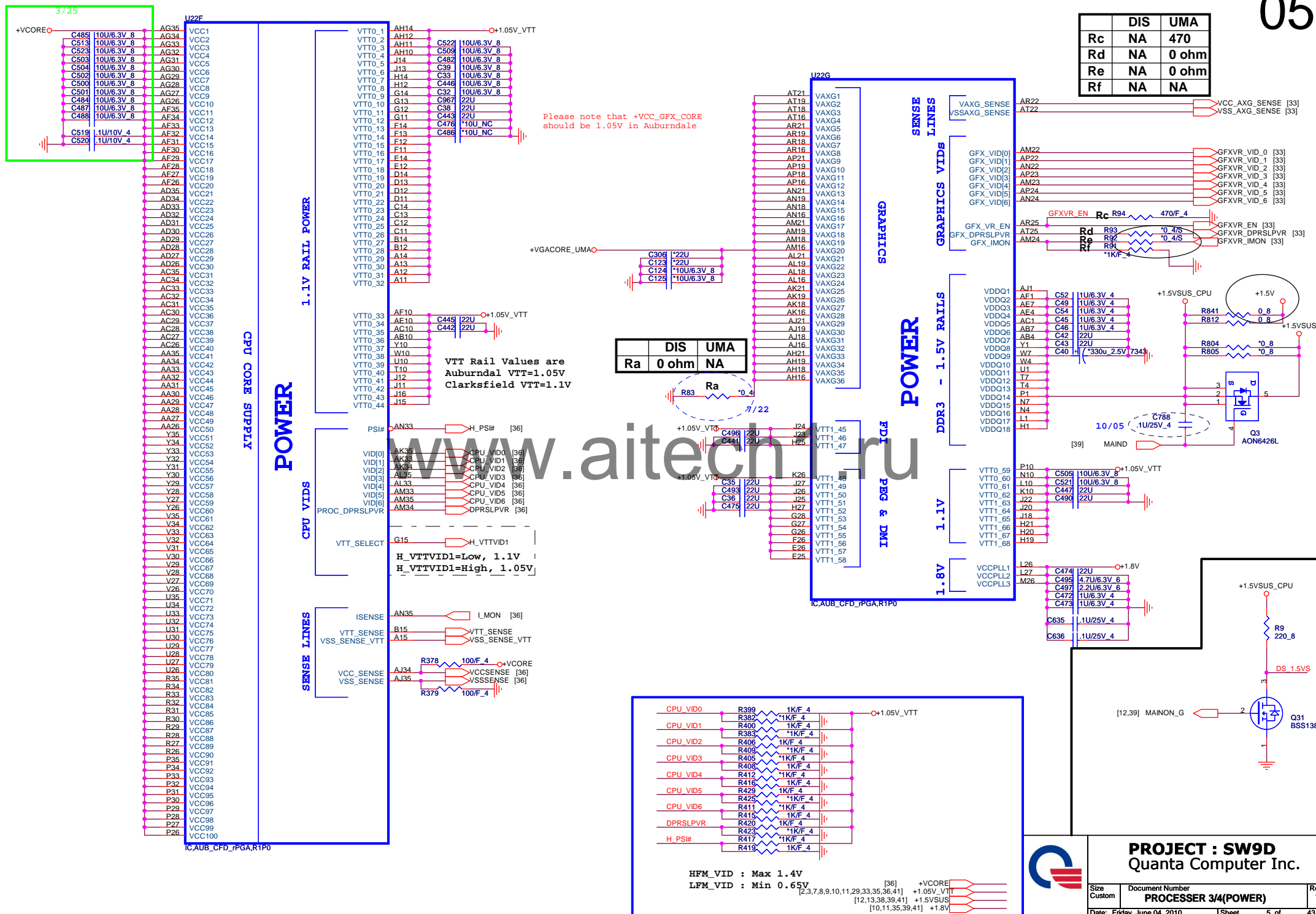
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



PROJECT : SW9D
Quanta Computer Inc.

Size Custom	Document Number PROCESSOR 2/4(DDR)	Rev 1A
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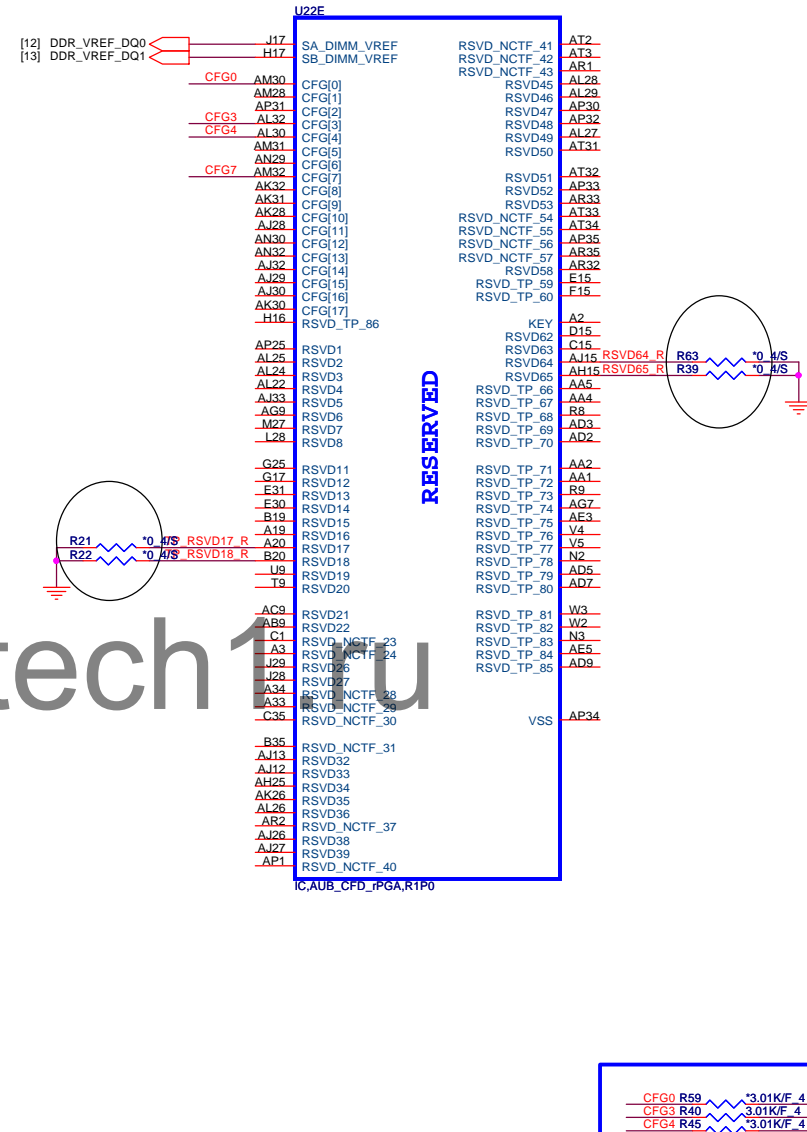
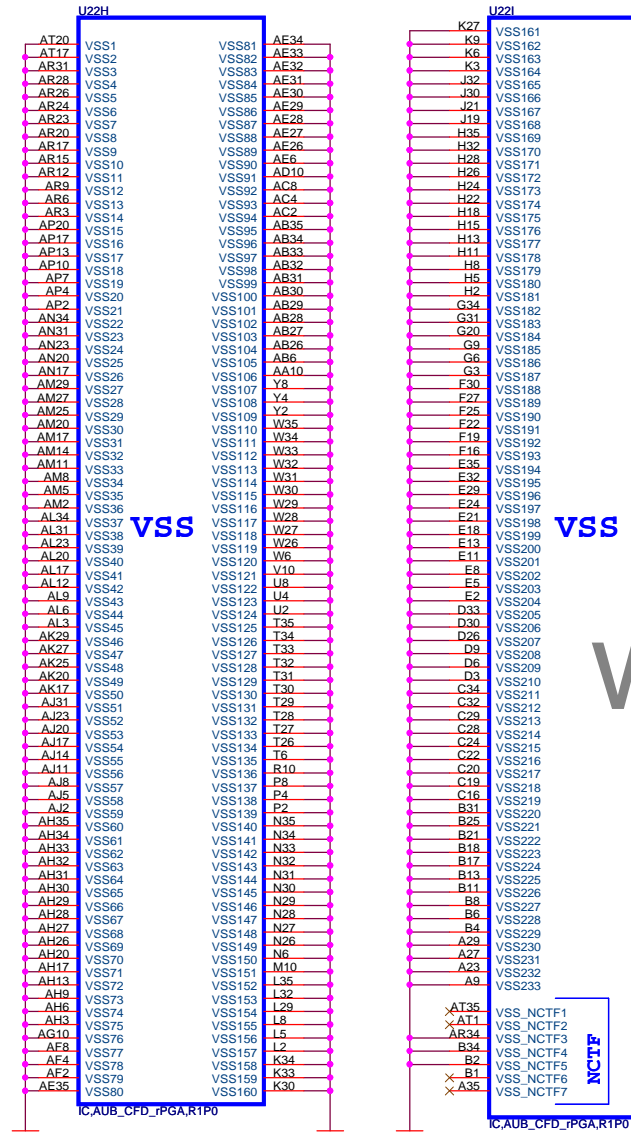
	DIS	UMA
Rc	NA	470
Rd	NA	0 ohm
Re	NA	0 ohm
Rf	NA	NA



AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

06



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1

For discrete only

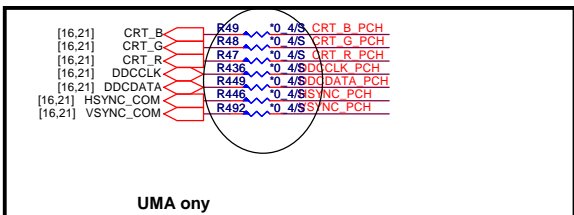
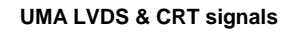
CFG0 R59 3.01K/F 4
CFG3 R40 3.01K/F 4
CFG4 R45 3.01K/F 4
CFG7 R52 3.01K/F 4

CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

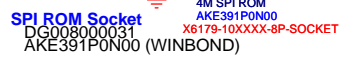
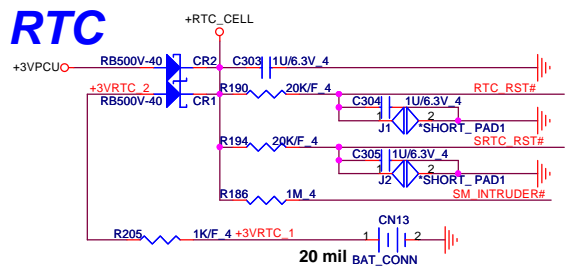
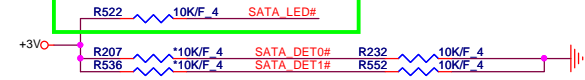
PROJECT : SW9D
Quanta Computer Inc.

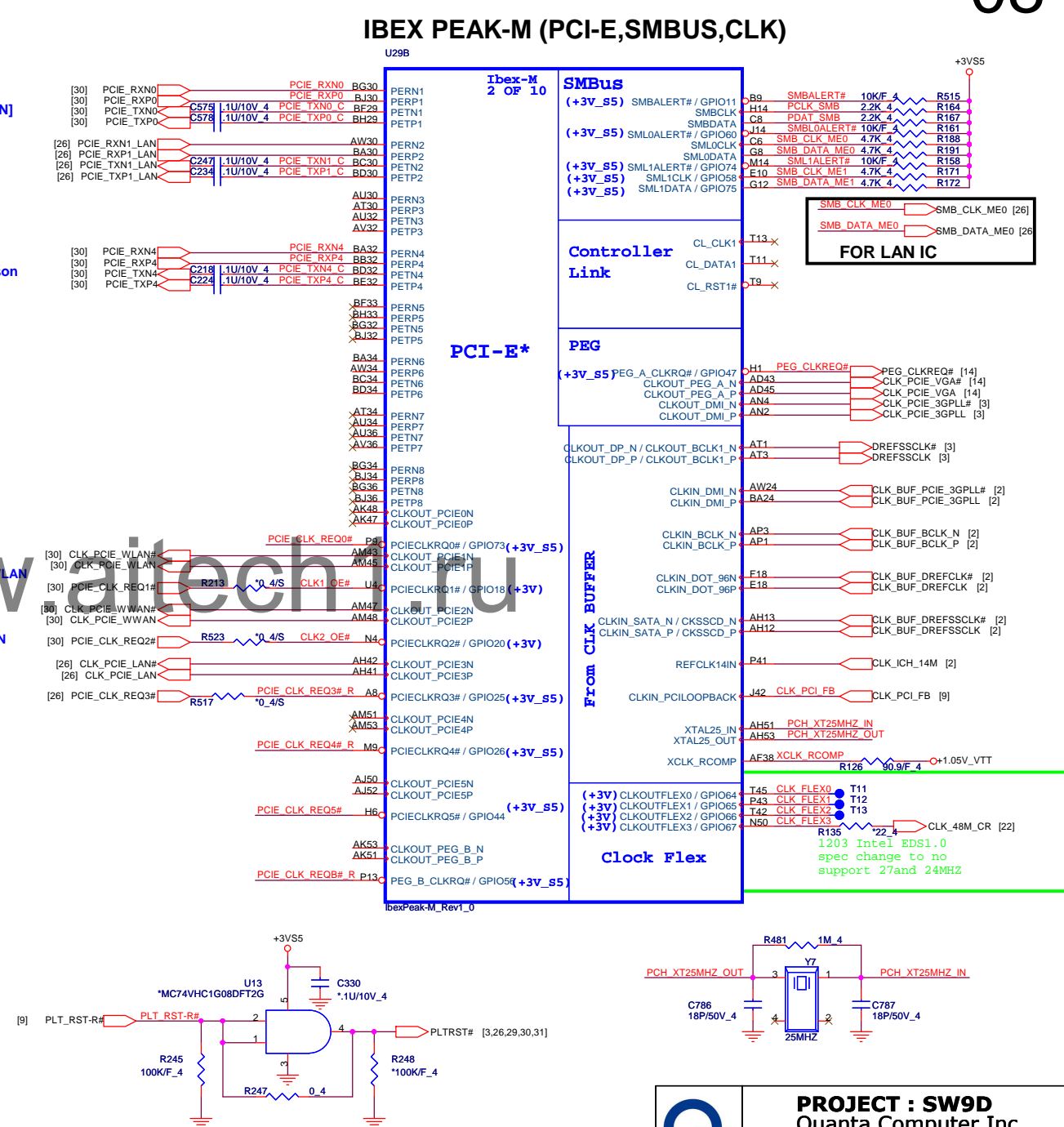
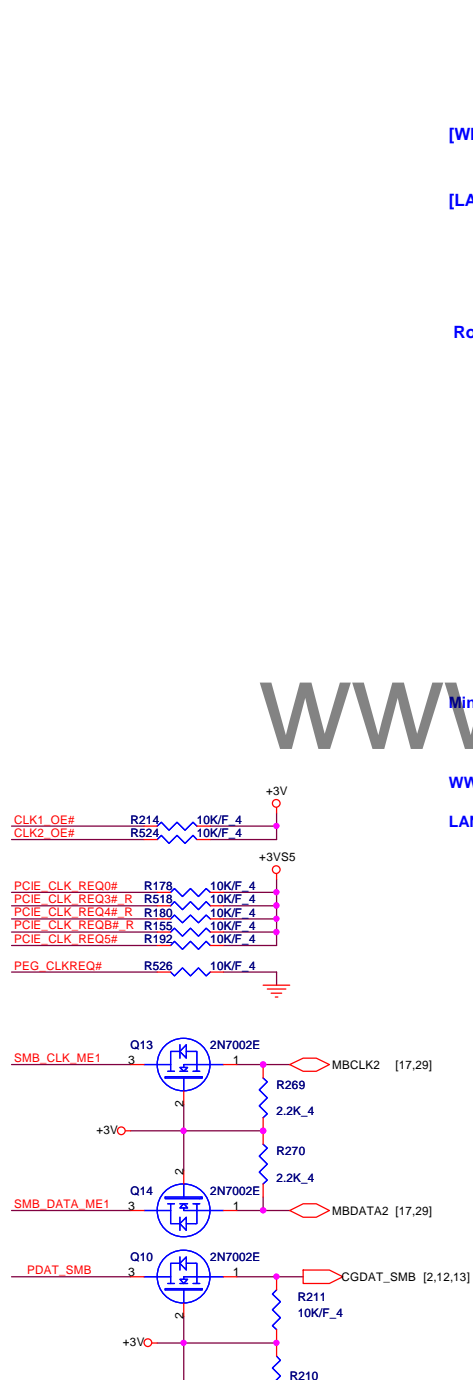
Size Custom Document Number
PROCESSOR 4/4(GND)

Date: Friday, June 04, 2010 Sheet 6 of 43

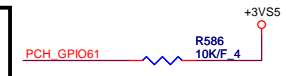


1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.





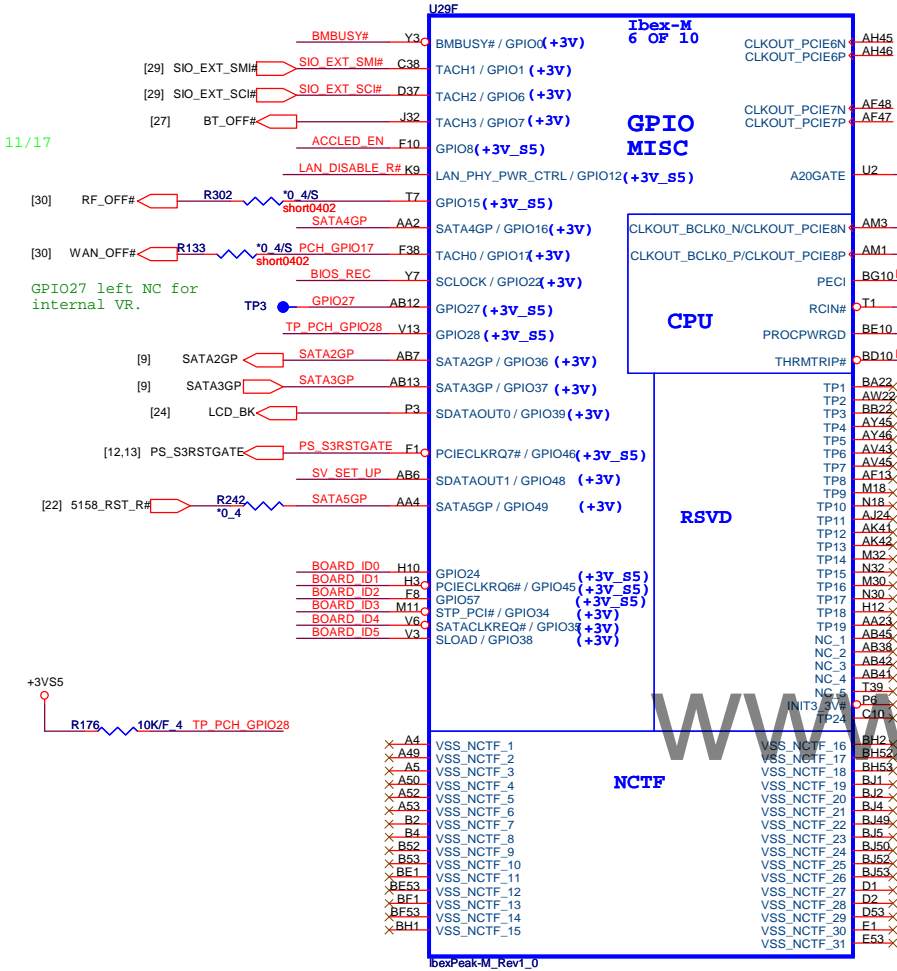
09



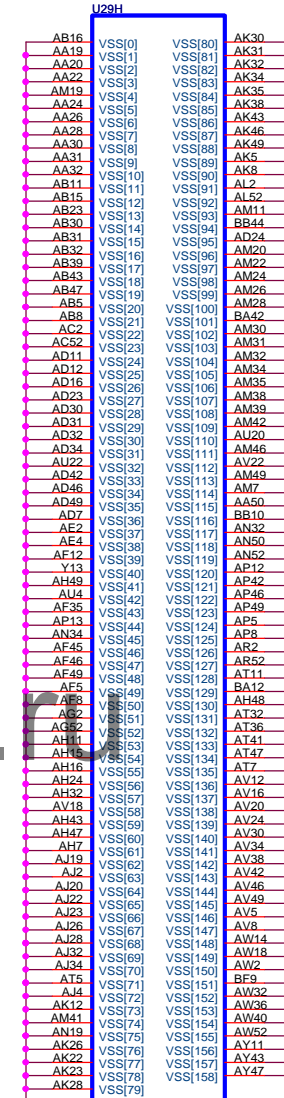
Discrete Only



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



10

Al6 swap override Strap/Top-Block Swap Override jumper

GNT3#

Low = Al6 swap override/Top-Block Swap Override enabled
High = Default

SV SET UP R198

SV_SET_UP

1-X High = Strong (Default)

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

NV_ALE NV_CLE

NV_ALE

NV_CLE

+1.8V

Danbury Technology Enabled

NV_ALE

High = Enable
Low = Disable

DMI Termination Voltage

NV_CLE

Set to Vcc when LOW
Set to Vcc/2 when HIGH

No Reboot Strap

PCH_GPIO33

BOARD ID SETTING

Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6
LG/CB	0=LG 1=CB						
UMA/Dis.		0=UMA 1=Dis.					
15.6"/ 14"			0=Q14/TW9 1=Q12/SW9				
MDC				0=YES 1=NO			
dobly					1=YES 0=NO		
OPTIMUS						1=YES 0=NO	

BIOS REC

BIOS RECOVERY
HIGH : DISABLE
LOW : ENABLE

PS S3RSTGATE R554

PCH GPIO17 R125

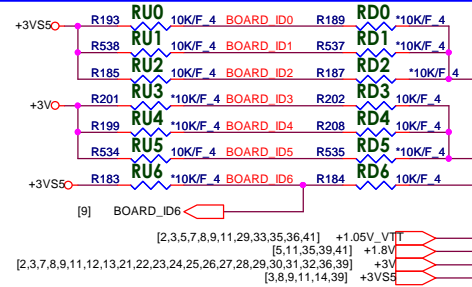
1204 (need to pull up to 3V from check list request)

ACCLED_EN R173

RF_OFF# R195

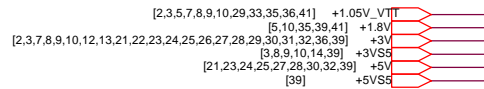
LAN_DISABLE_R# R181

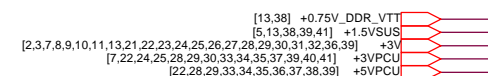
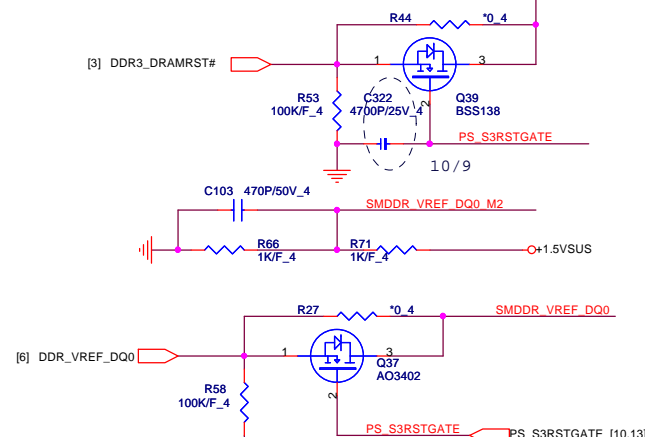
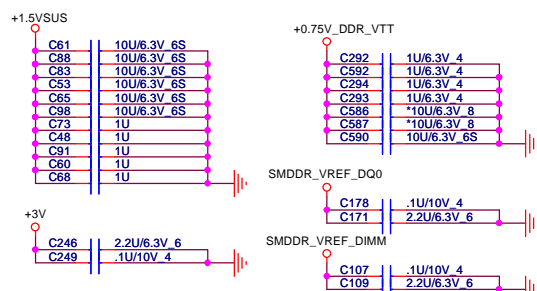
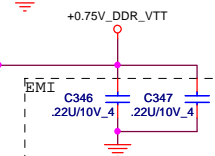
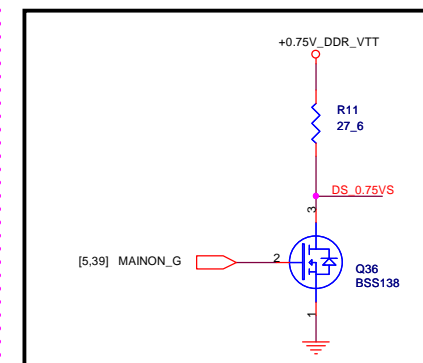
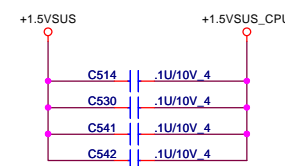
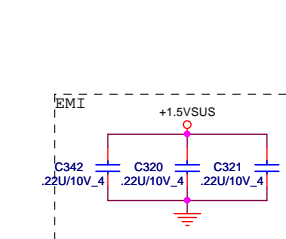
1204 (need to pull up to 3V_S5 from check list request)



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Place these Caps near So-Dimm1.

+1.5VSUS

- C64 10U/6.3V 6S
- C71 10U/6.3V 6S
- C75 10U/6.3V 6S
- C85 10U/6.3V 6S
- C44 10U/6.3V 6S
- C80 10U/6.3V 6S
- C72 1U
- C47 1U
- C77 1U
- C62 1U
- C57 1U

+0.75V_DDR_VTT

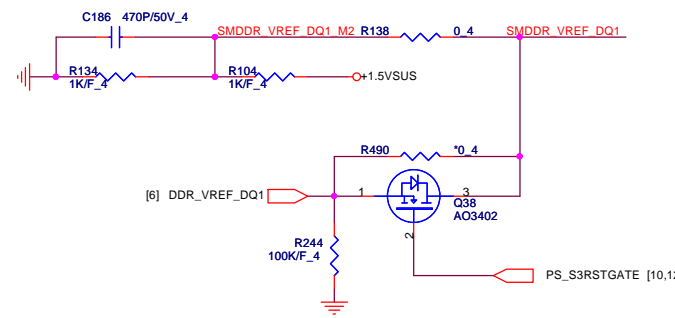
- C258 1U/6.3V 4
- C591 1U/6.3V 4
- C257 1U/6.3V 4
- C259 1U/6.3V 4
- C251 1U/6.3V 8
- C589 10U/6.3V 6S
- C260 10U/6.3V 6S






+3V

- C245 2.2U/6.3V 6
- C248 1U/10V 4
- C108 1U/10V 4
- C96 2.2U/6.3V 6

SMDDR_VREF_DIMM

SMDDR_VREF_DQ1

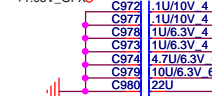


		[12,38]	+0.75V_DDR_VTT	
		[6,12,28,39,41]	+1.5VSUS	
[2,3,7,8,9,10,11,12,21,22,23,24,25,26,27,28,29,30,31,32,36,39]			+3V	
[27,22,24,25,28,29,33,34,35,37,39,40,41]			+3VPCU	
[22,28,29,33,34,35,36,37,38,39]			+5VPCU	

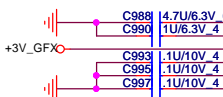
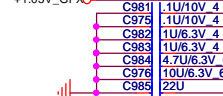
PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD > 2.2A

U67A
FCBGA973-NVIDIA-N11P-ES-A1
COMMON

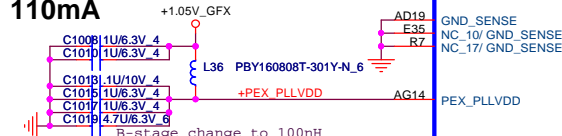
+1.05V_GFXO ~ 500mA



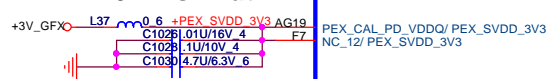
+1.05V_GFX 1600mA



12~16 mils width
110mA

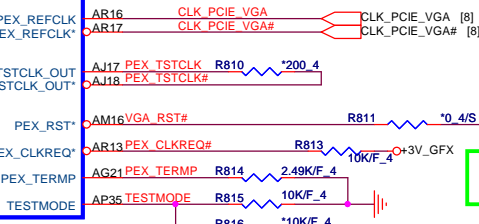
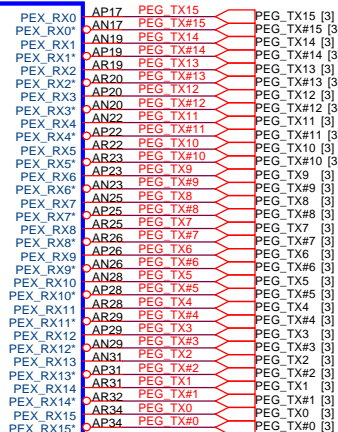


12~16 mils width

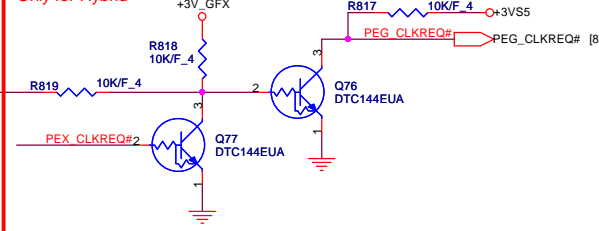


AG20 PEX_CAL_PU_GND/ NC
A2 NC_1
AB7 NC_2
AD6 NC_3
AF6 NC_4
AG6 NC_5
AJ5 NC_6
AK15 NC_7
AL7 NC_8
E7 NC_11
H32 NC_13
P6 NC_15
U7 NC_18
V6 NC_19

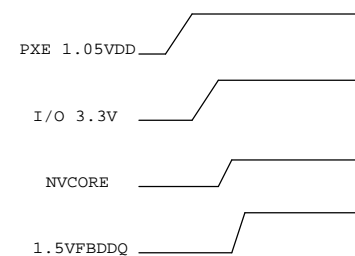
PCI EXPRESS



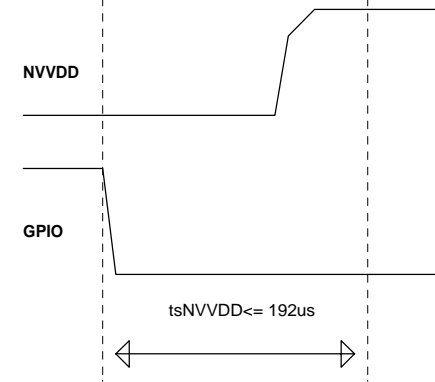
Only for Hybrid



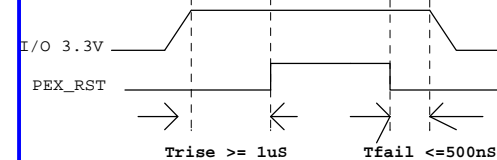
power up sequence



NB9M: VGACORE +0.90V (Normal) , +1.09V
NVVDD Maximum Settling Time



PEX_RST timing

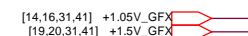


[15,16,31,41] +1.05V_GFX
[16,17,31,32,37,41] +3V_GFX

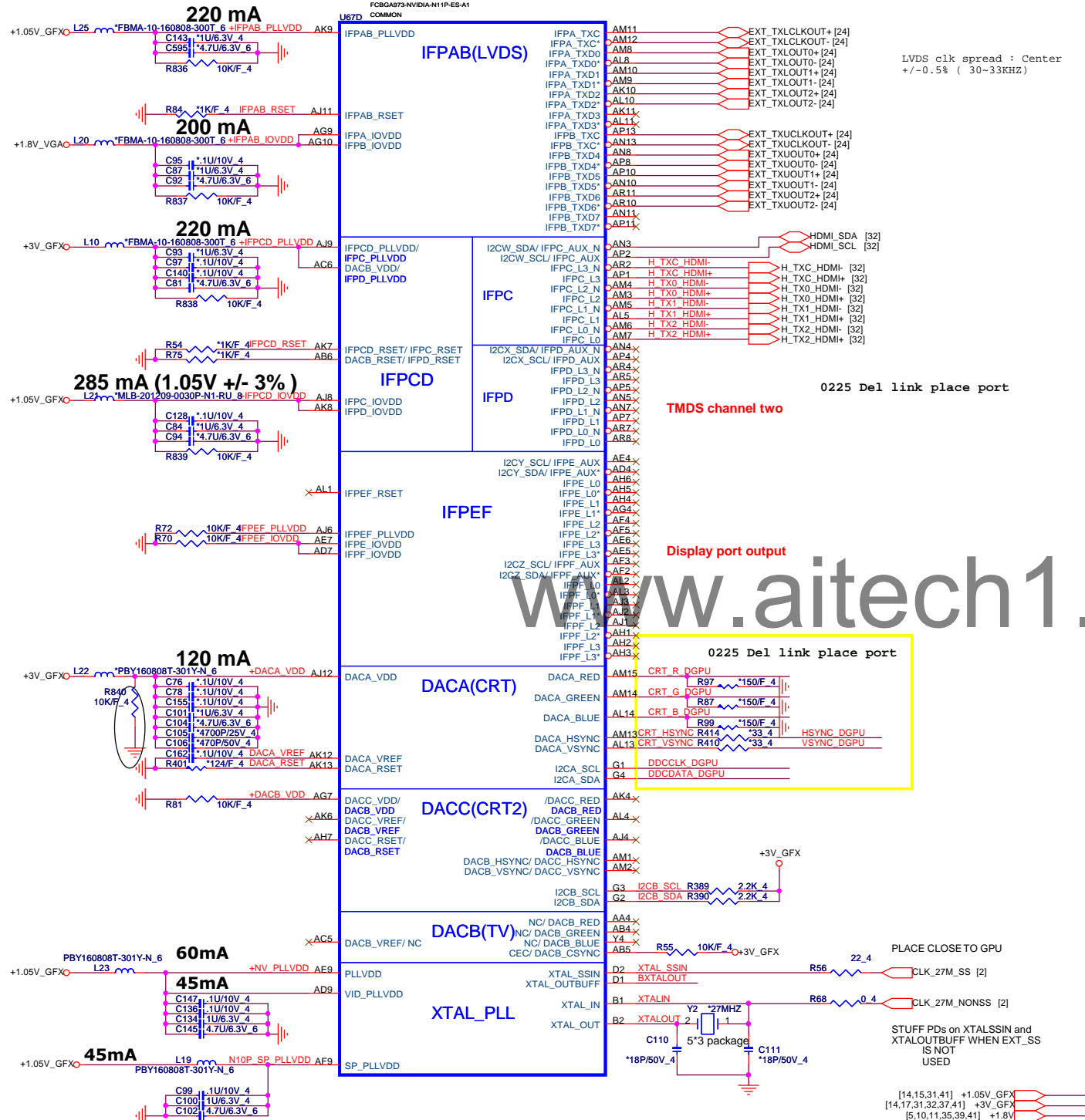


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220 mA



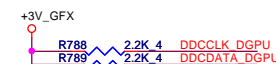
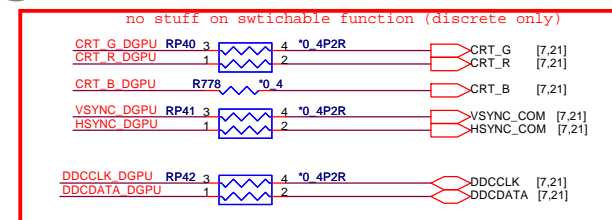
LVDS clk spread : Center
+/-0.5% (30~33KHZ)

0225 Del link place port

TMD5 channel two

Display port output

0225 Del link place port



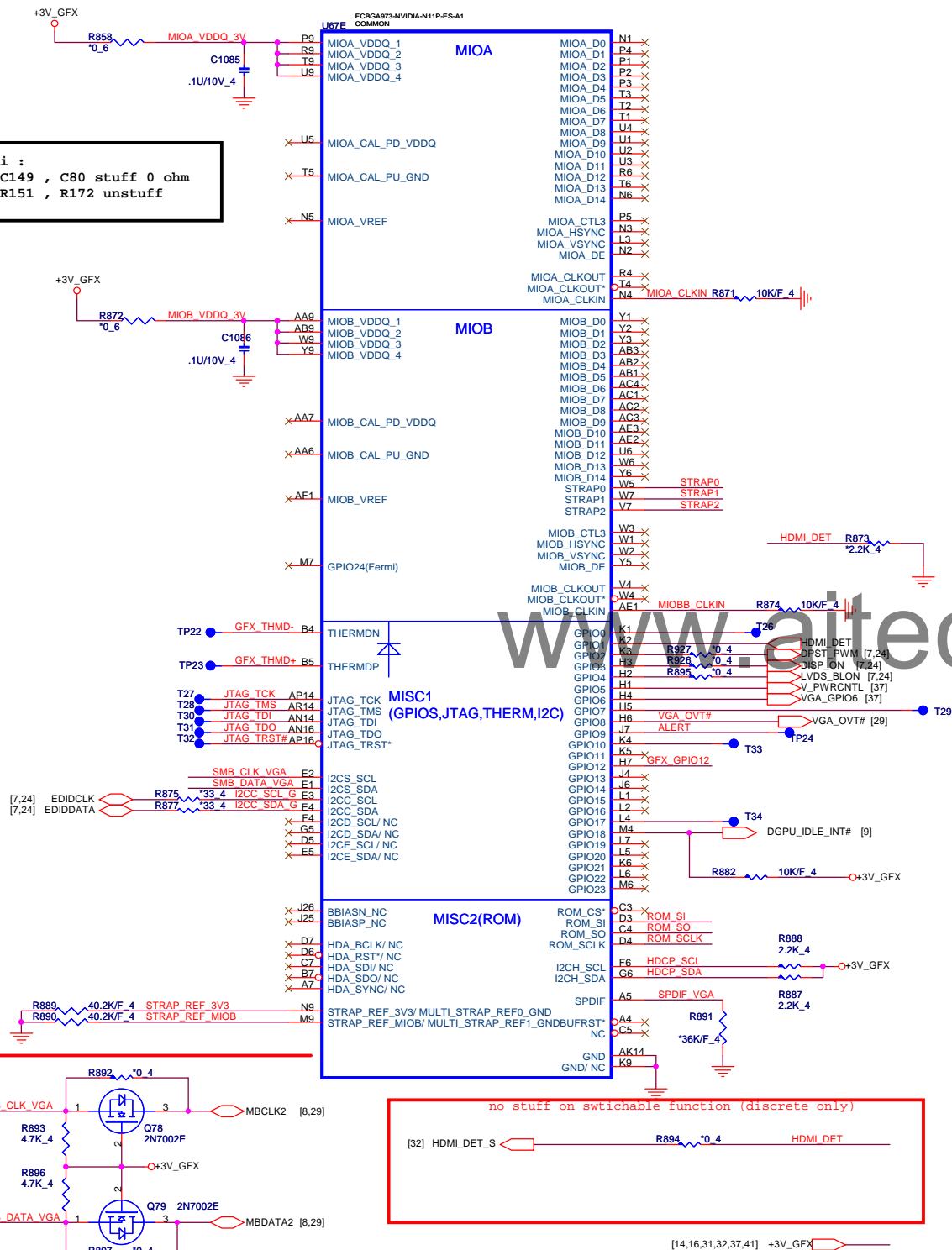
10 k Ω pull-down only if no spread chip used.



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Fermi :
1 : C149 , C80 stuff 0 ohm
2 : R151 , R172 unstuff

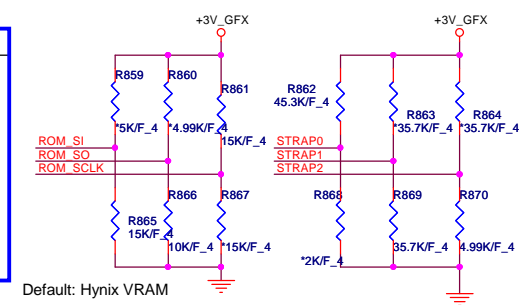


N11P-GE ES (ID=>0DFE)
STRAP2 PU-VDD 35K
ROM_SCLK PU-VDD 15K

N11P-GE QS=>0DF0
STRAP2 PD-GND 5K
ROM_SCLK PU-VDD 15K

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



Default: Hynix VRAM

4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1% (0402)]
10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1% (0402)]
35.7K/F 4: CS33572FB18 [RES CHIP 35.7K 1/16W +1% (0402)]
45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]

20K/F 4: CS32002FB29 RES CHIP 20K 1/16W +1% (0402)

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Reserved	IDGH1G-04A1F1C-16X	PD 10K
0001	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Qimonda	H5TQ1G63BFR-12C	PD 15K
0010	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Hynix	K4W1G1646E-HC12	PD 20K
0011	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Samsung		
0101		Reserved		
0110				
XXXX	DDR3 64Mx16x8, 128bit, 1GB, 667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB, 667MHz	Samsung	K4W1G1646D-EC12	

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2 ^{11/13}
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL ^{11/13}
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

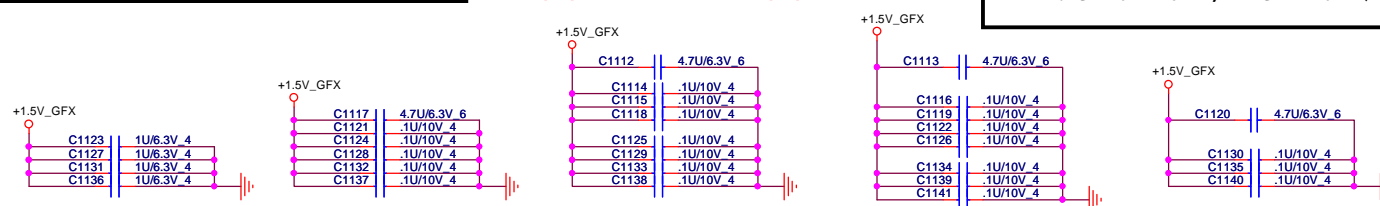
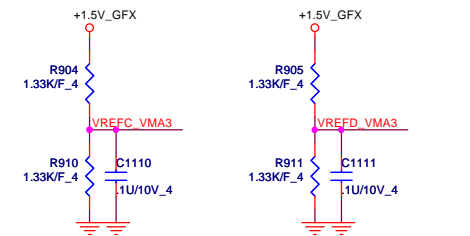
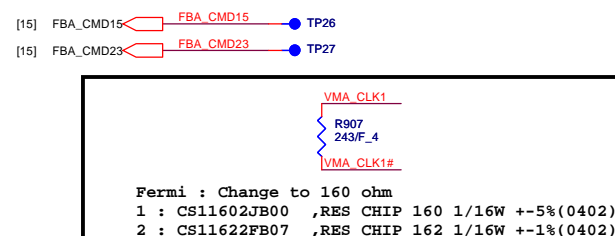
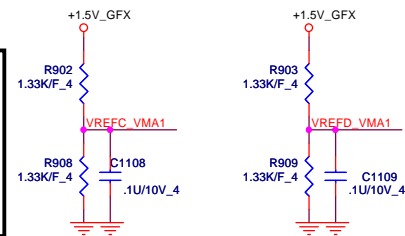
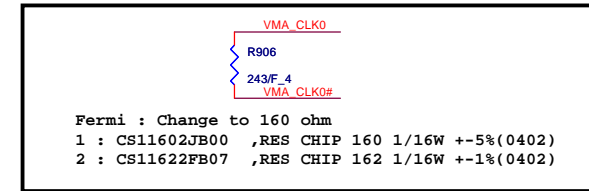


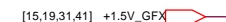
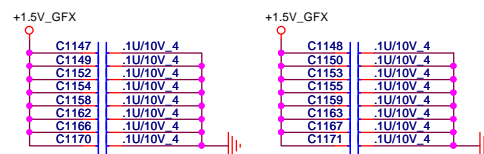
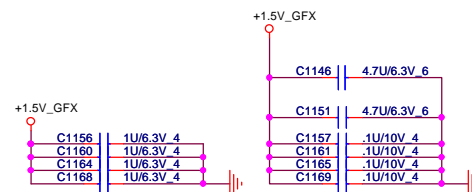
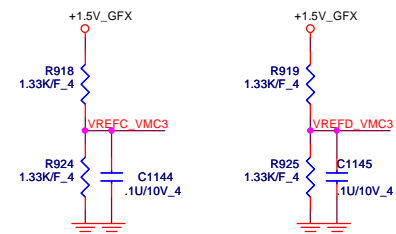
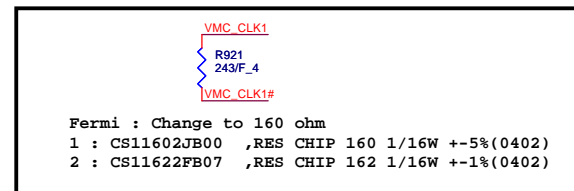
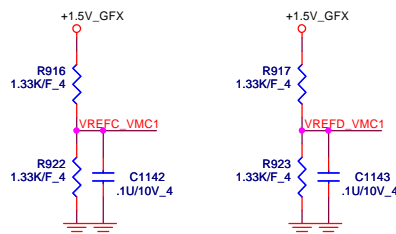
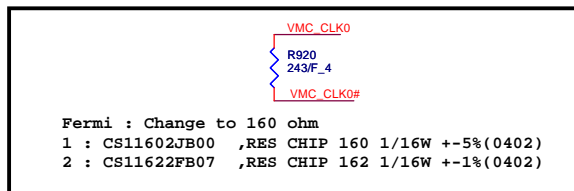
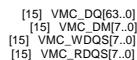
PROJECT : SW9D
Quanta Computer Inc.

Size Custom	Document Number N11x-Fermi	Rev 1A
Date: Friday, June 04 2010	Sheet 8 17 of 43	



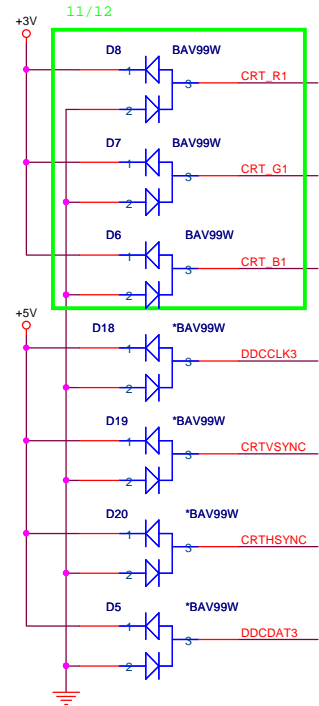
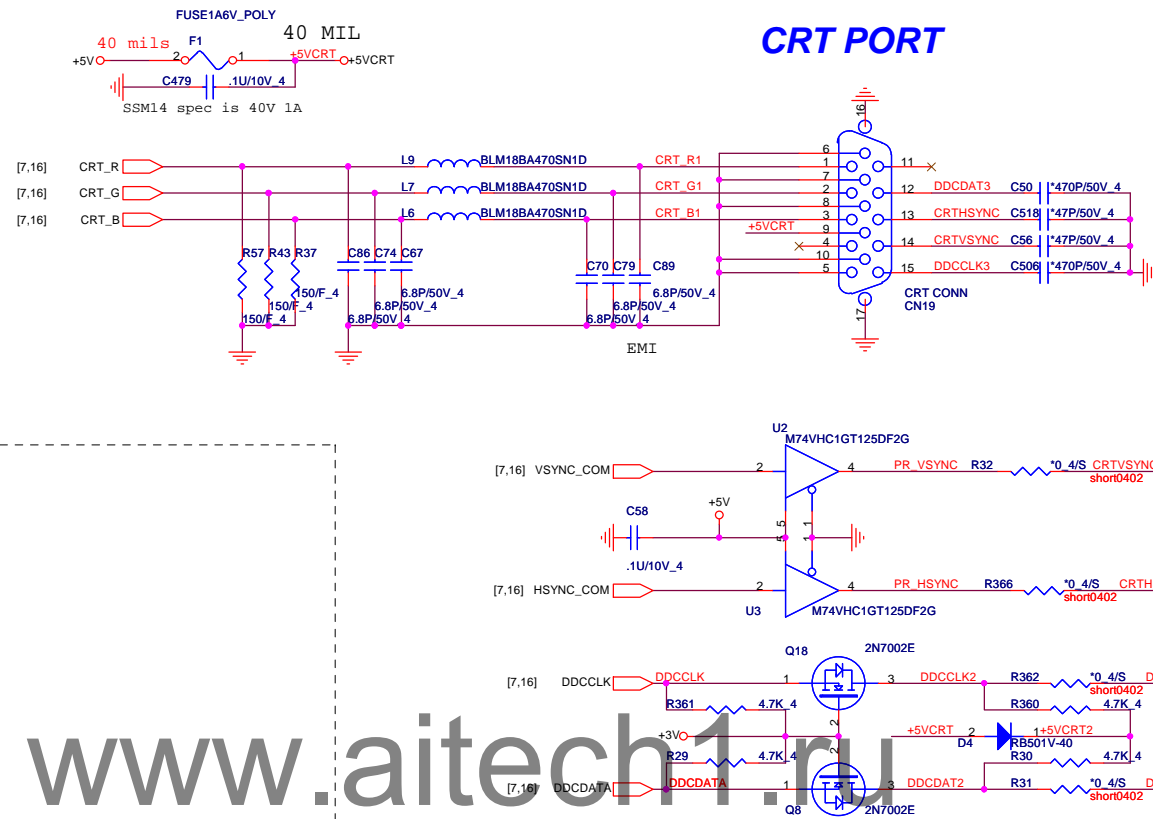
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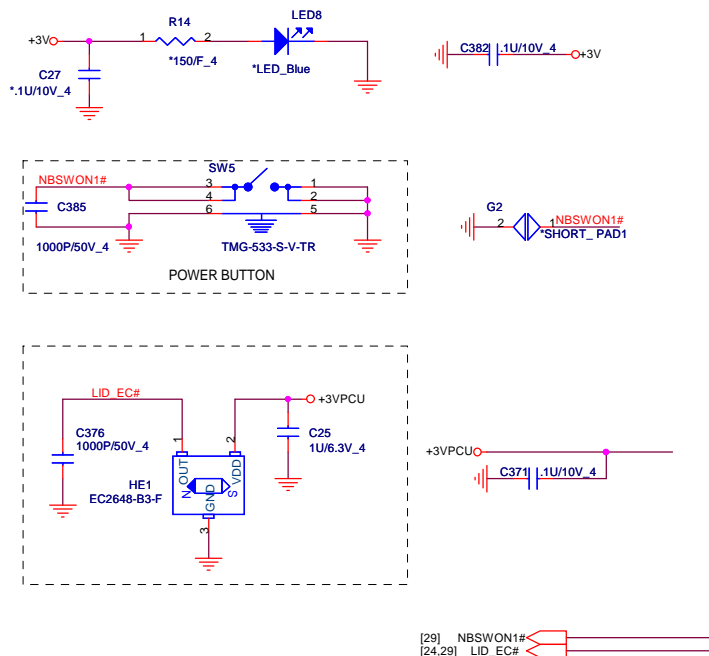
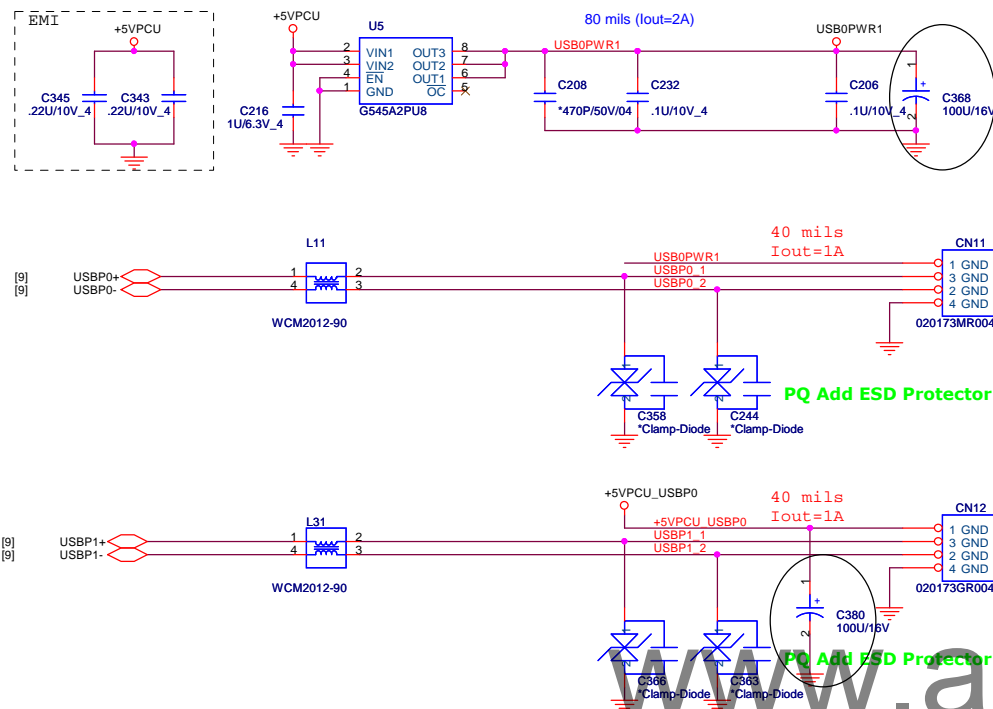
PROJECT : SW9D
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USB CONNECTOR

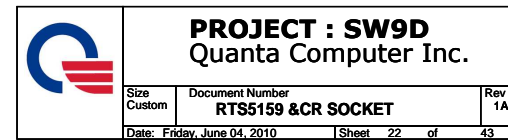
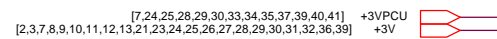
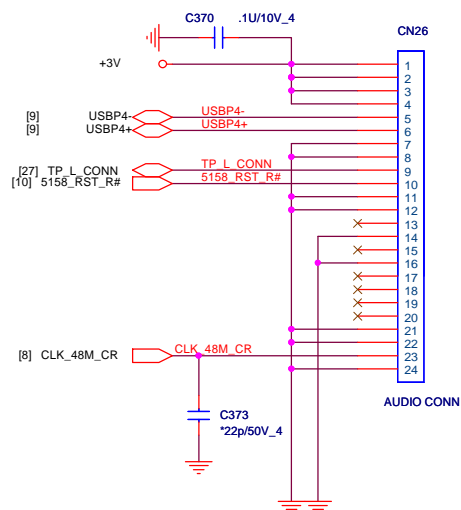


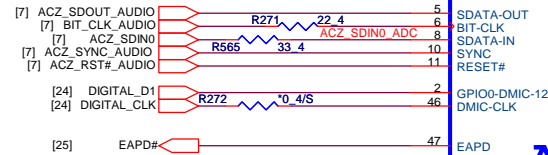
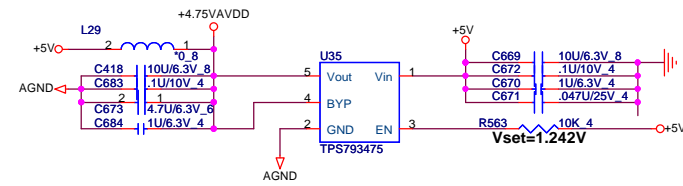
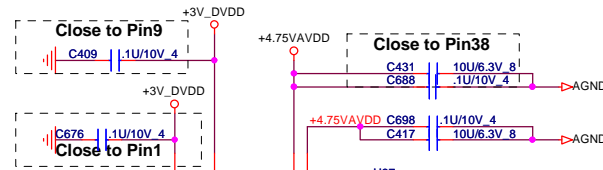
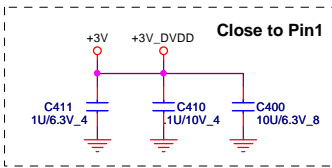
22

1. NBSW01
2. GND
3. GND
4. LID_EC#
5. +3V
6. +3VPCU

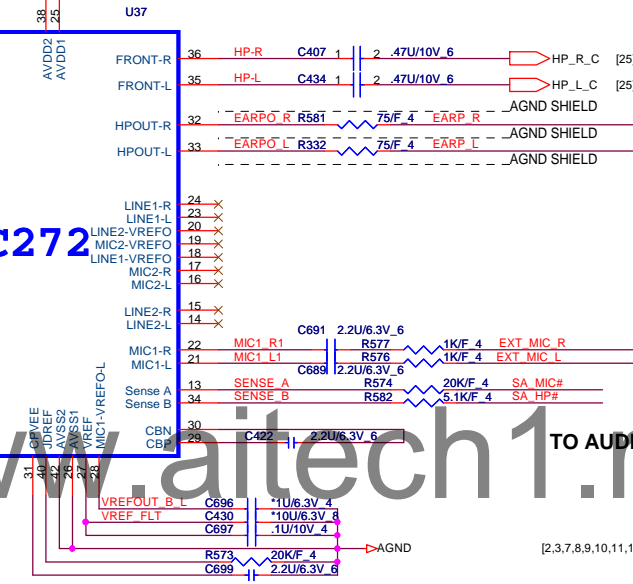
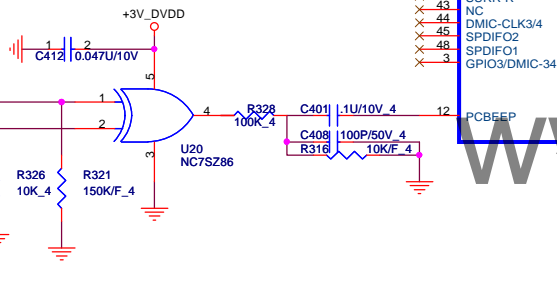
TO M/B CON.

PV Change CN2 footprint 88501-2001-24p-l-nb5

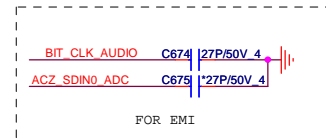




ALC272

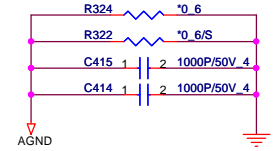


To Internal Speakers



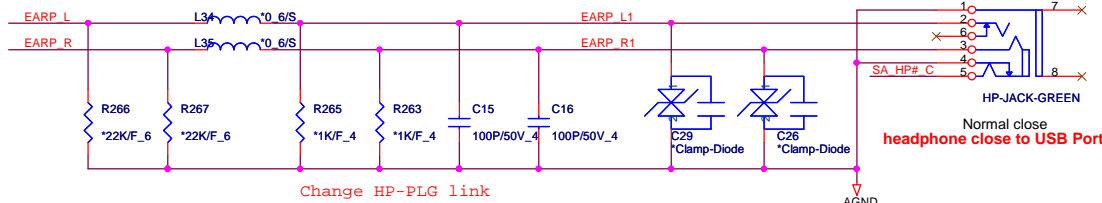
TO Audio Jack MIC

TO AUDIO/B CON.

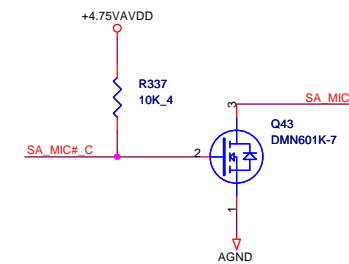
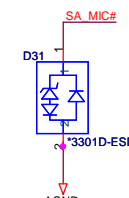
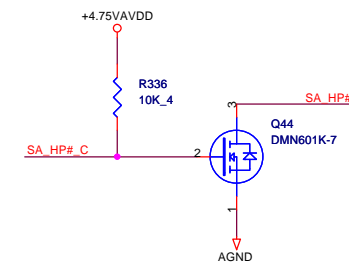
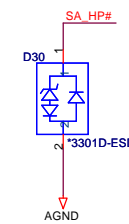
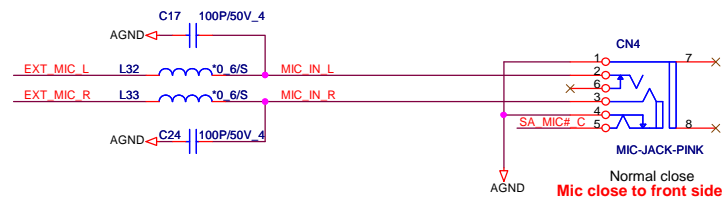


AUDIO CONNECTOR

10/07

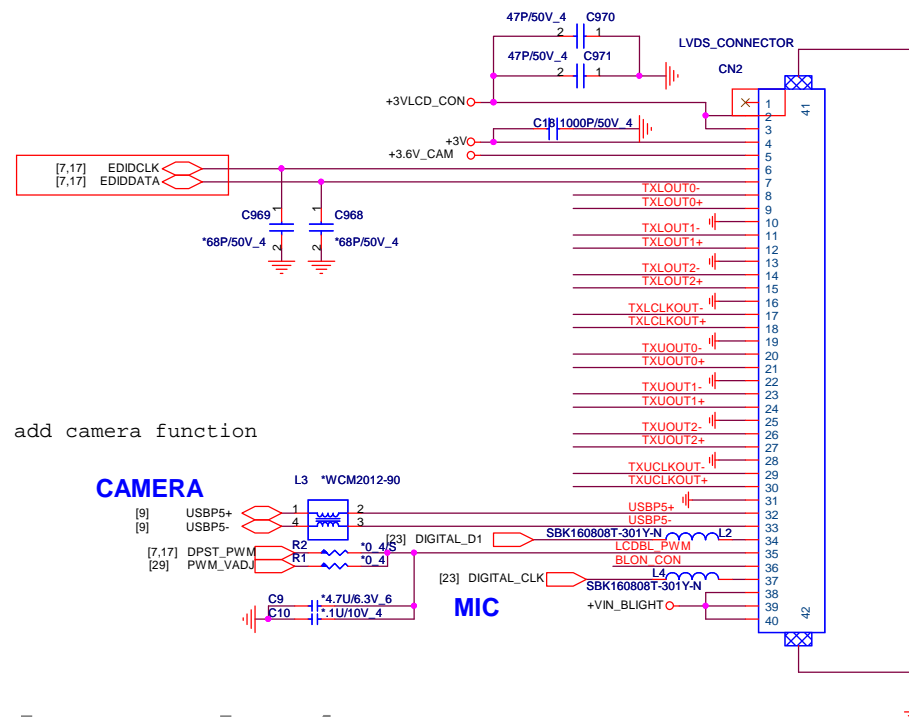
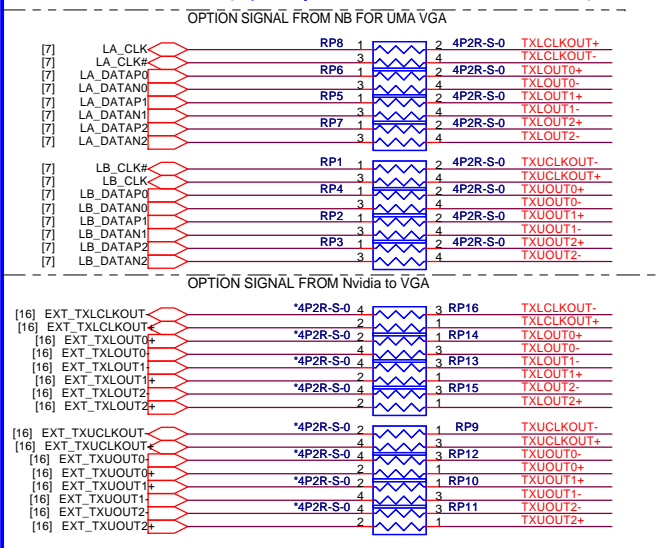


AUDIO JACKS CHANGE TO NORMAL OPEN



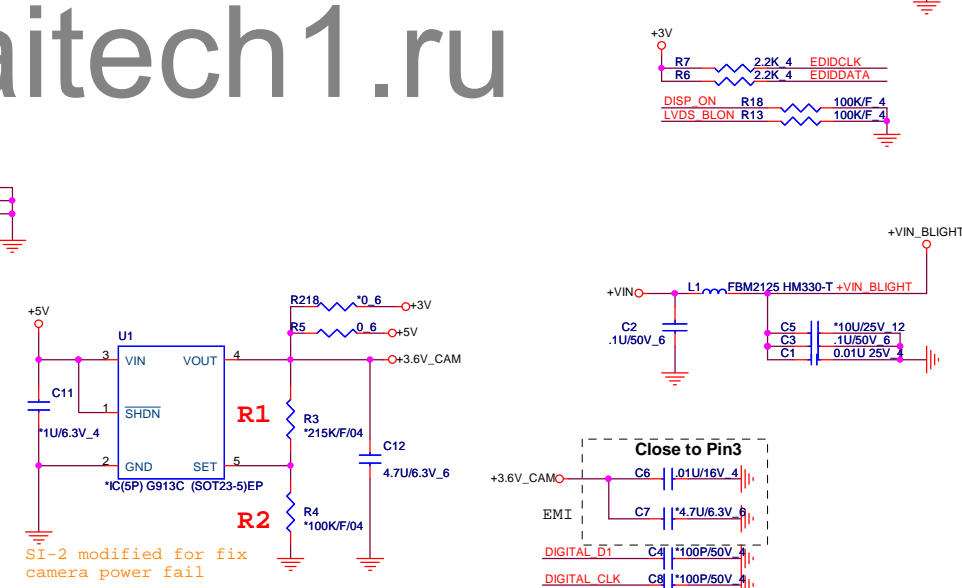
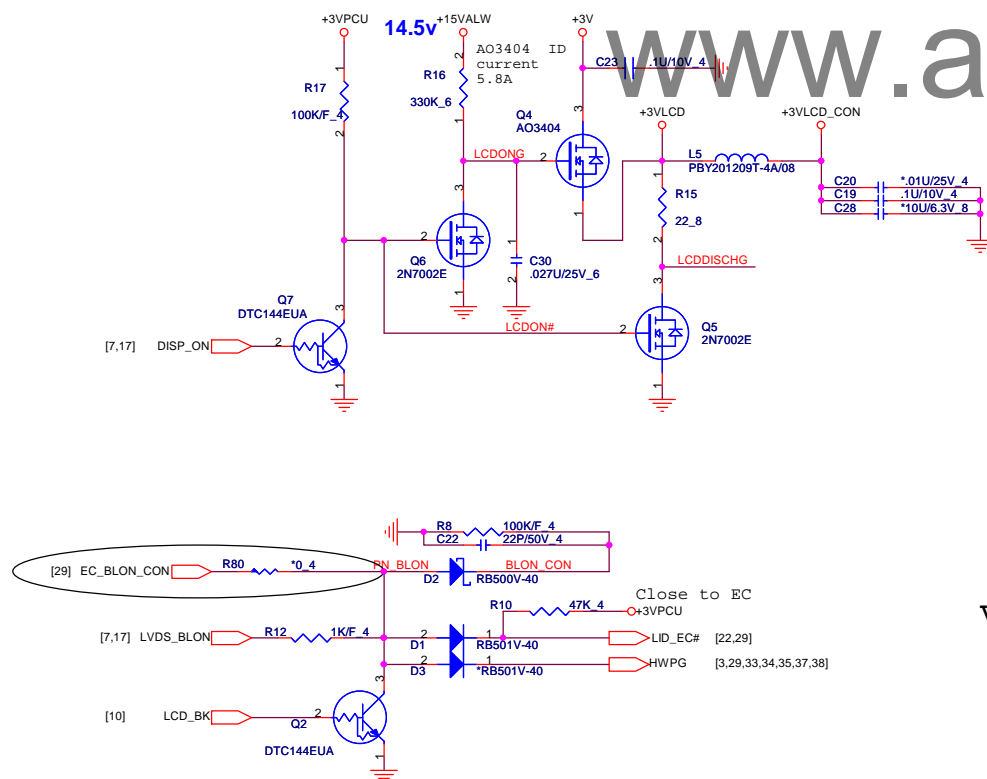
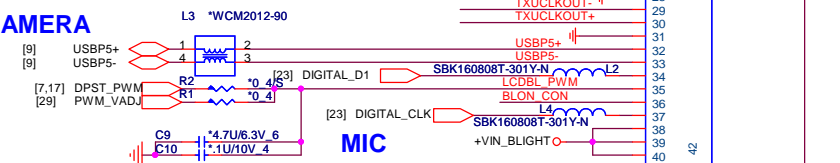
PROJECT : SW9D
Quanta Computer Inc.

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

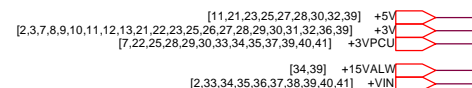


```
0820 add camera function
```

CAMERA

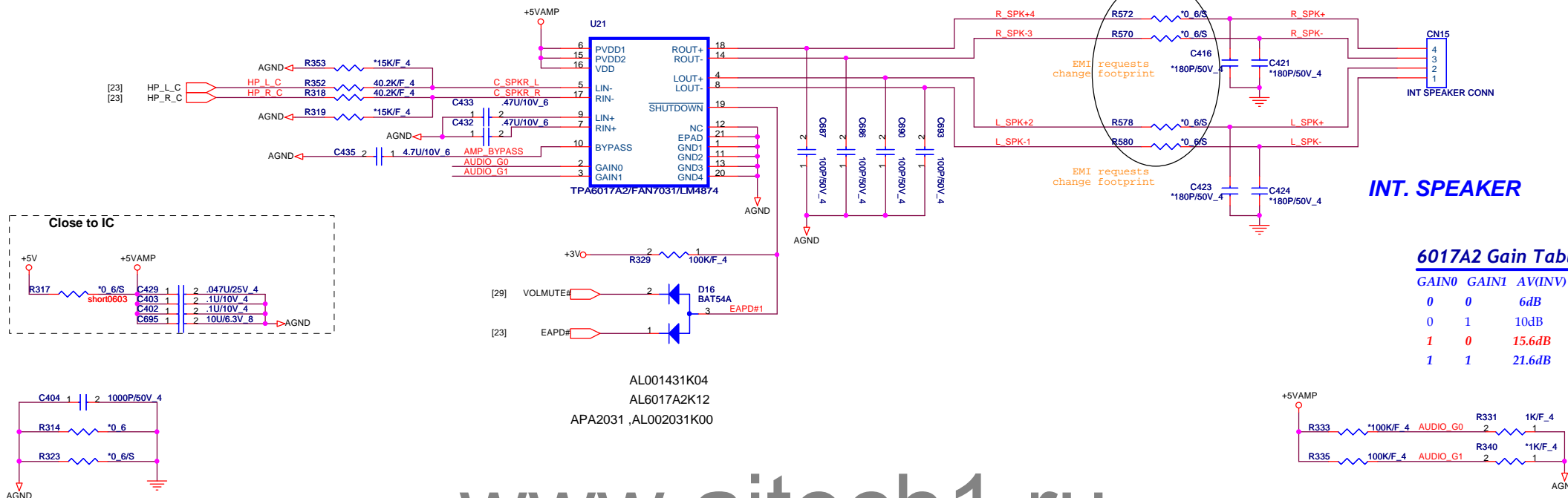


$$V_{out} = 1.25(1 + R_1/R_2)$$

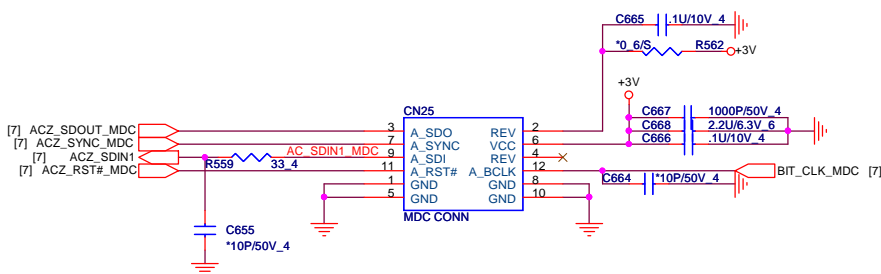


AUDIO AMPLIFIER

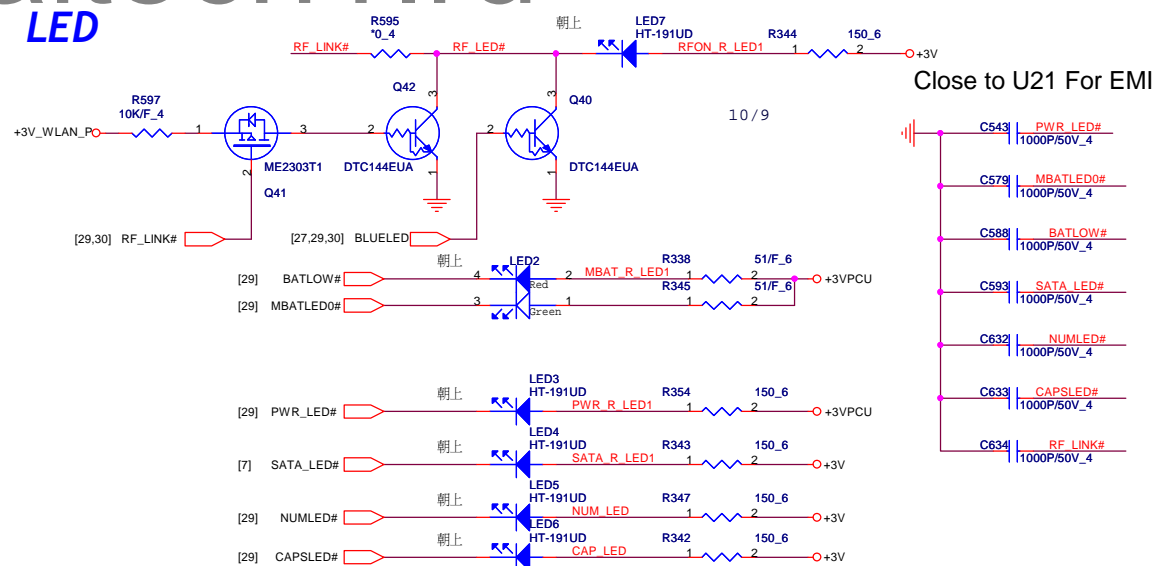
25



MDC CONNECTOR



LED

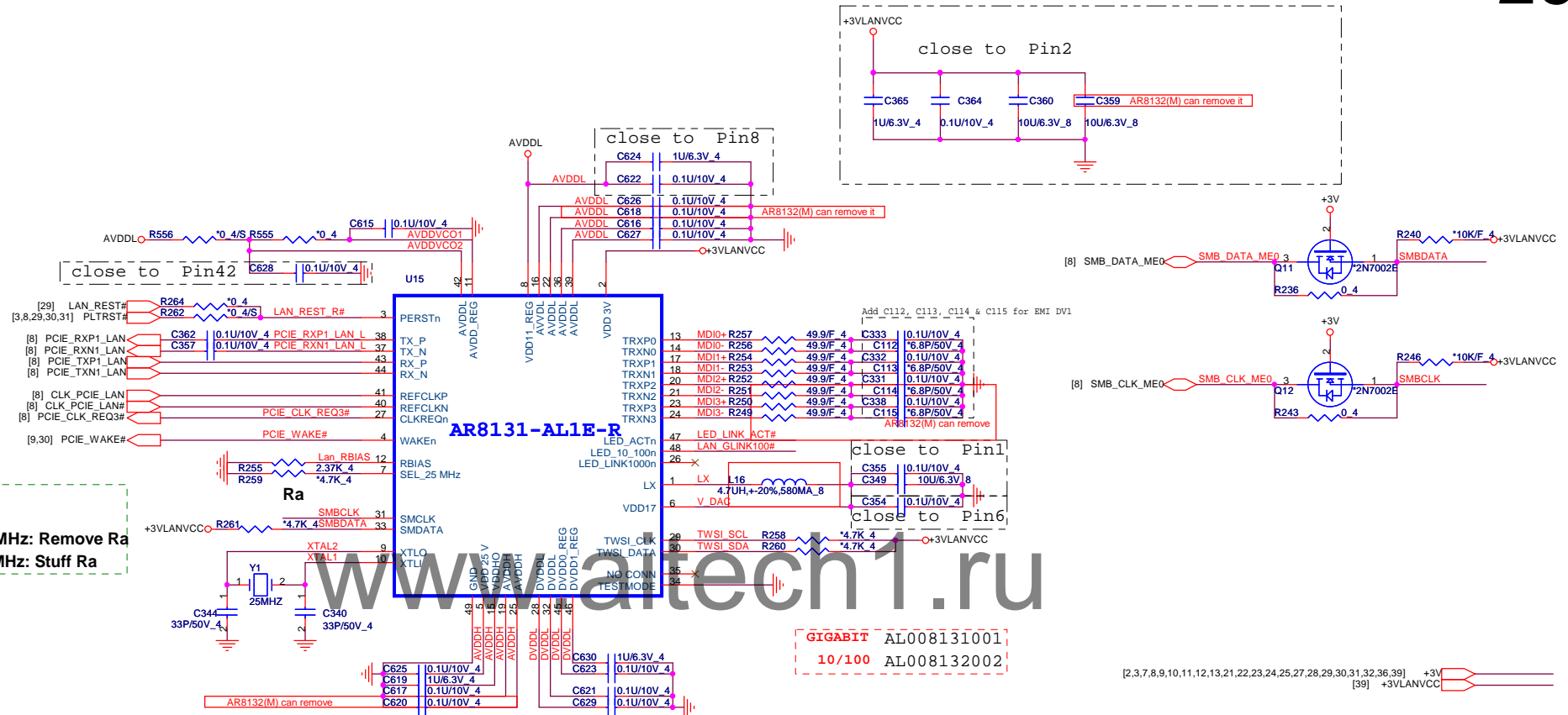


PROJECT : SW9D
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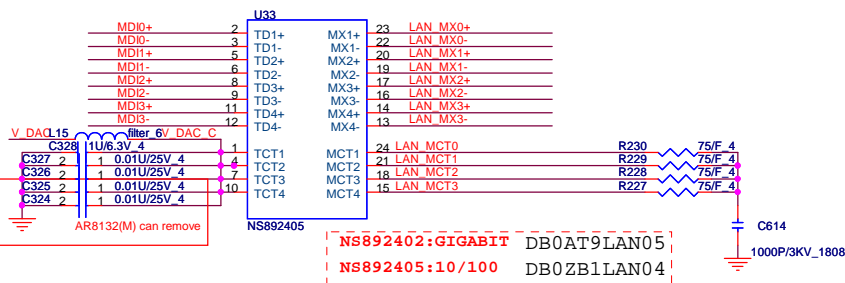
[11,21,23,24,27,28,30,32,39] +5V
[7,22,24,28,29,30,33,34,35,37,39,40,41] +3VPCU
[2,3,7,8,9,10,11,12,13,21,22,23,24,26,27,28,29,30,31,32,36,39] +3V

Clock Resource

For AR8131/M Input 25MHz: Remove Ra
For AR8131/M Input 48MHz: Stuff Ra

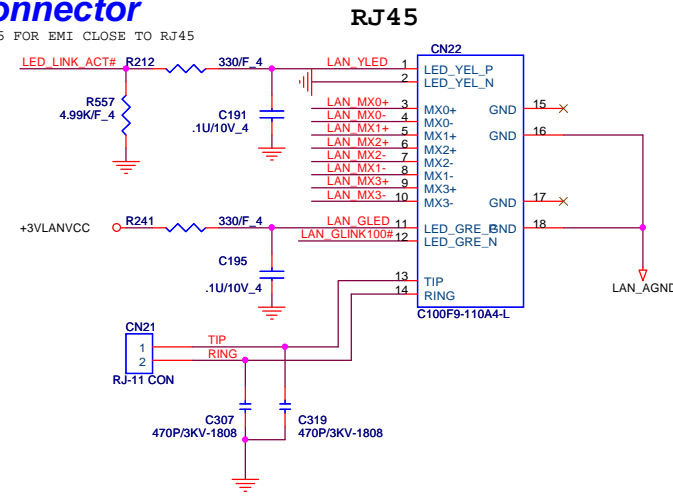


Transformer for 10/100/1000



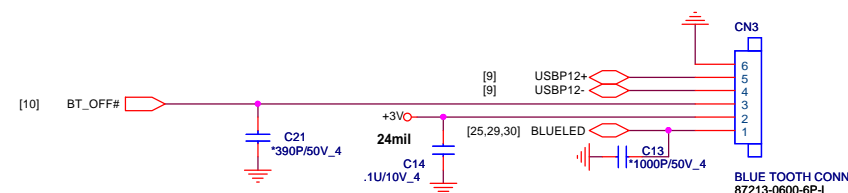
Lan Connector

C105,C135 FOR EMI CLOSE TO RJ45

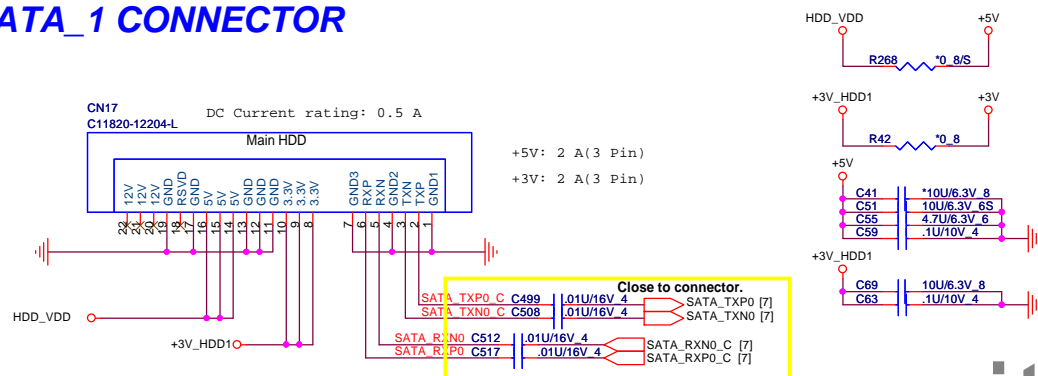


PROJECT : SW9D
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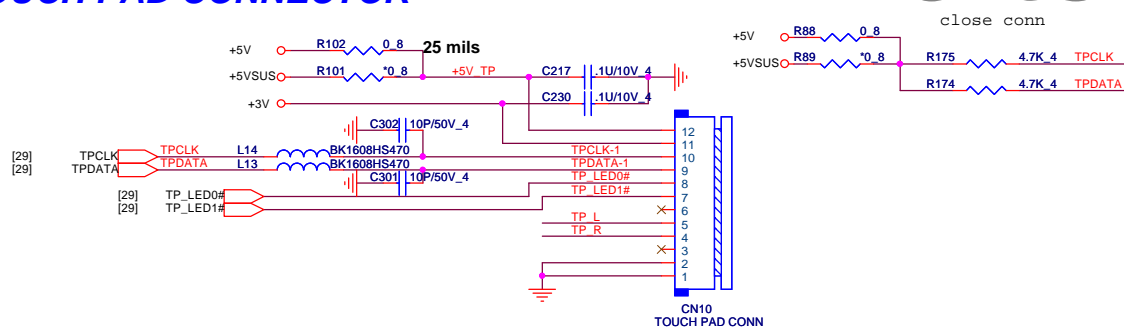
Size	Document Number	Rev
Custom	AR8131(M)/RJ45	1A
Date: Friday, June 04, 2010	Sheet 26 of 43	



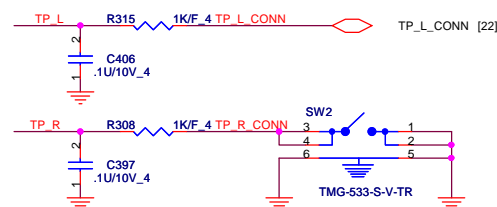
SATA_1 CONNECTOR



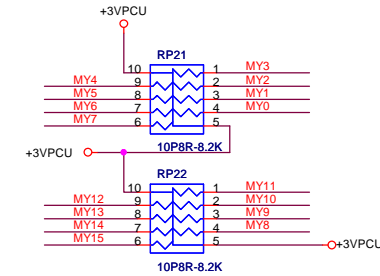
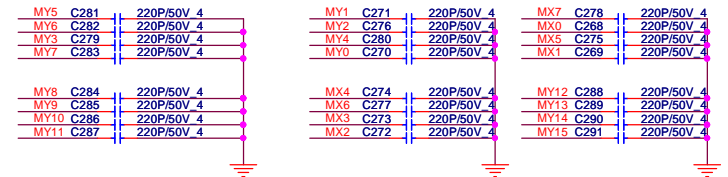
TOUCH PAD CONNECTOR



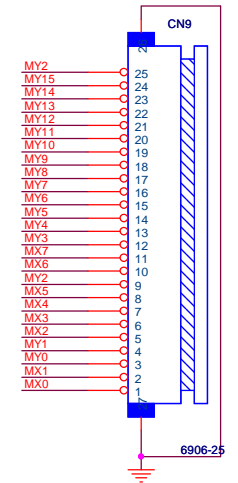
TOUCH PAD L/R SW1,SW2 in QL2 use, SW3,SW4 in SW9 use



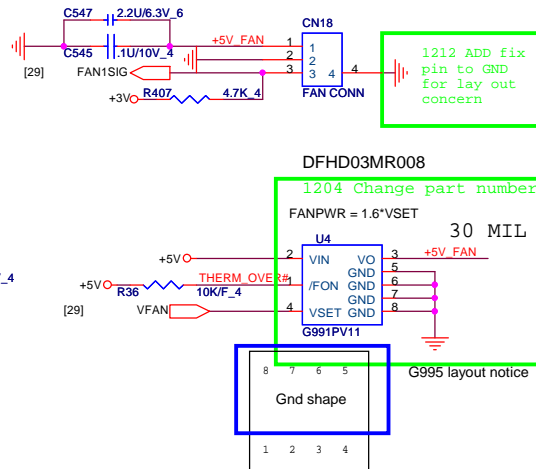
KEYBOARD Con.



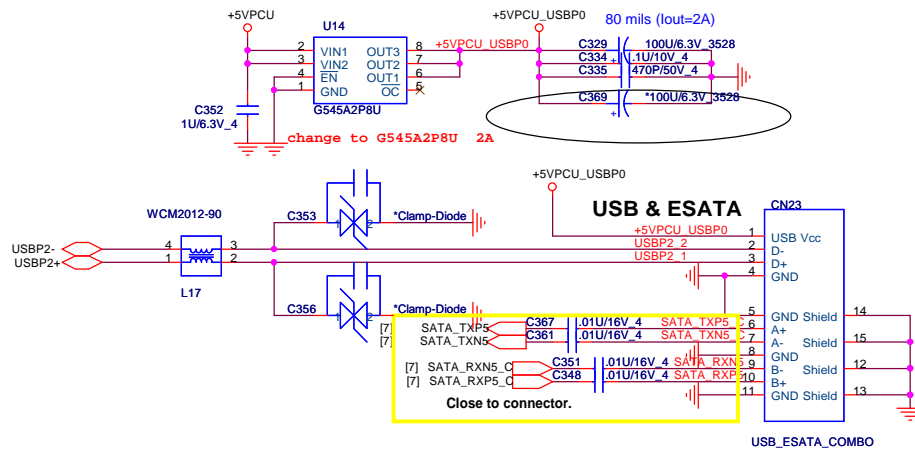
[29] MY[0..15] MY[0..15]
[29] MX[0..7] MX[0..7]



CPU FAN



E-SATA/USB COMBO



Capacity board Con.

[11,21,23,24,25,27,30,32,39] +5V
[2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,29,30,31,32,36,39] +3V
[7,22,24,25,29,30,33,34,35,37,39,40,41] +3VPCU
[22,29,33,34,35,36,37,38,39] +5VPCU



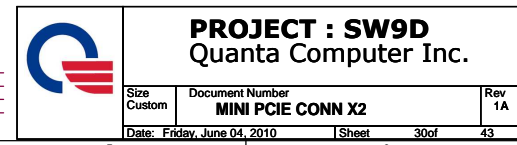
PROJECT : SW9D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/PWR/ESATA/FAN/CAM/MIC	1A
Date: Friday, June 04, 2010	Sheet 28 of 43	

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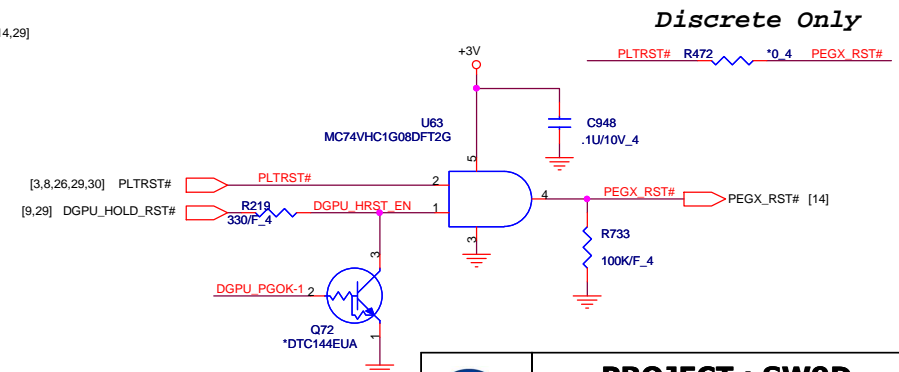
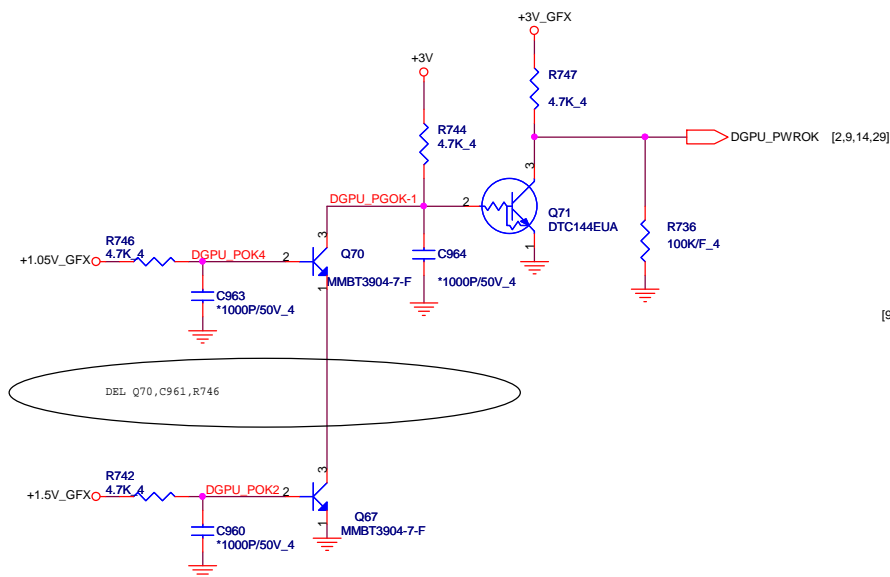


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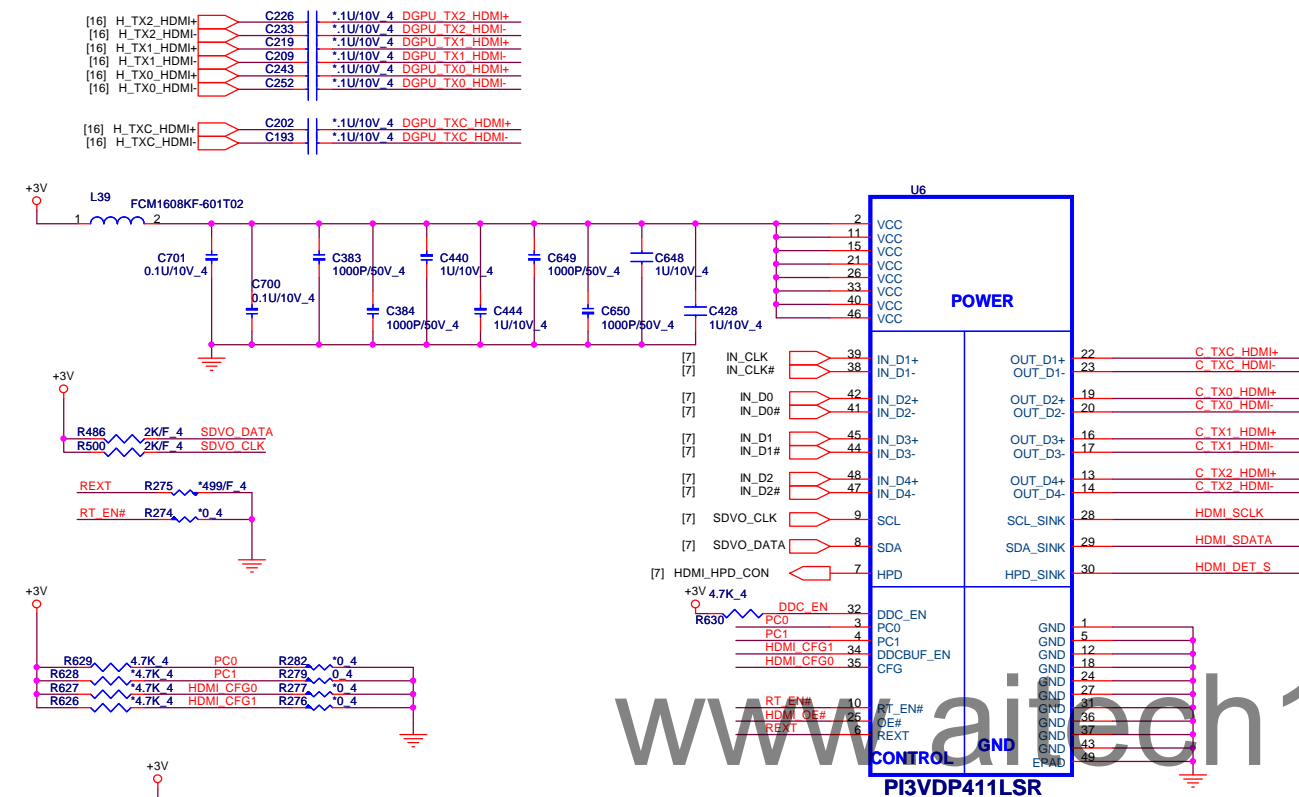
SEL	FUNCTION
LOW	DGPU
HIGH	IGPU



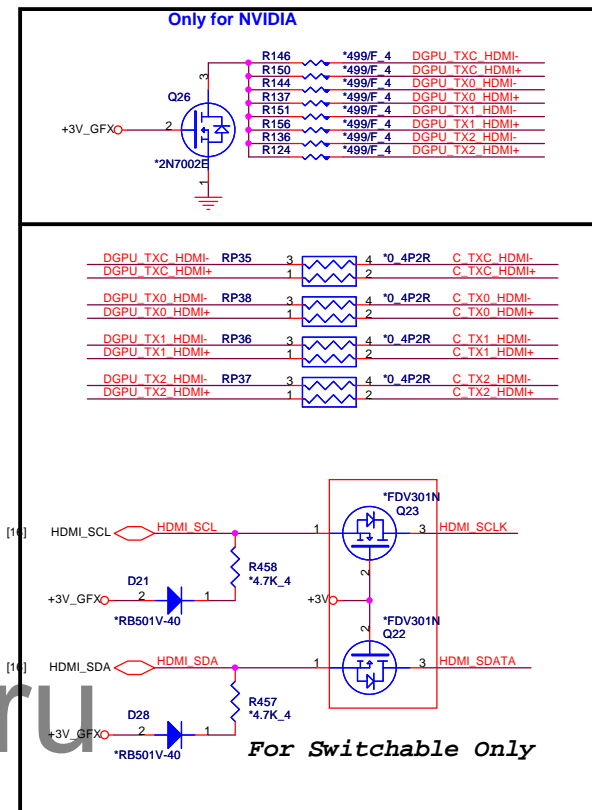
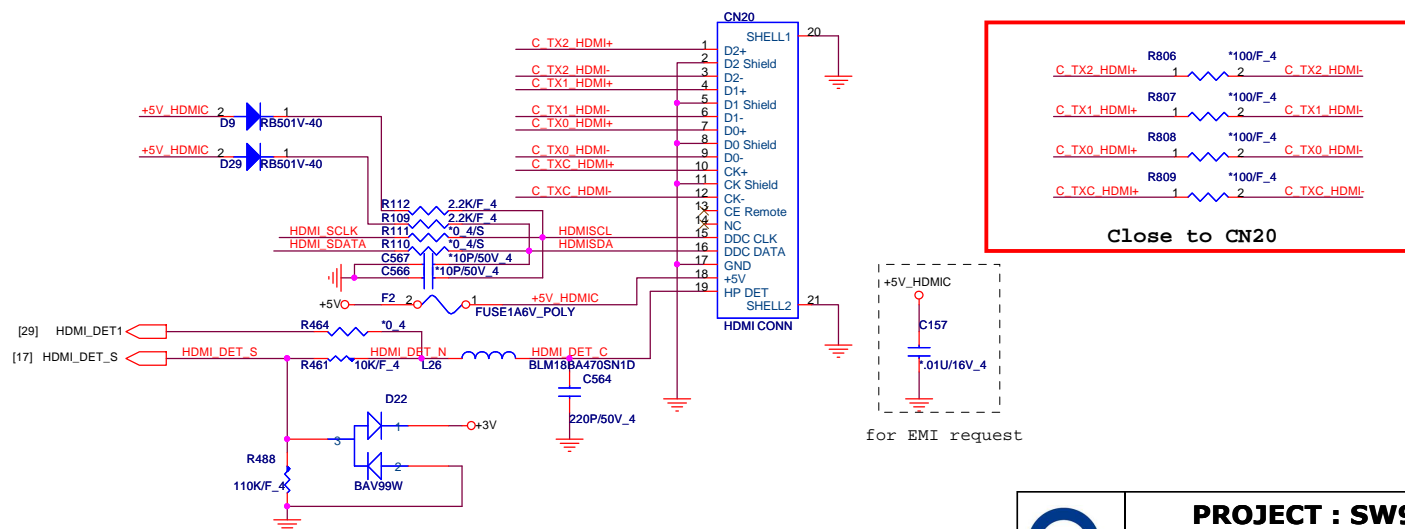
PROJECT : SW9D
Quanta Computer Inc.

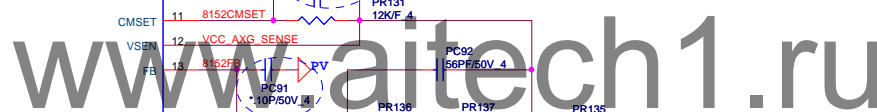
Size Custom	Document Number LVDS / CRT Switch	Rev 1A
Date: Friday, June 04, 2010	Sheet 31 of 43	

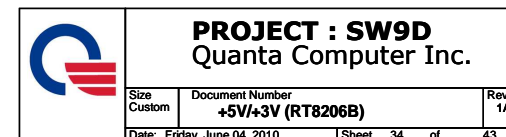
DGPU HDMI

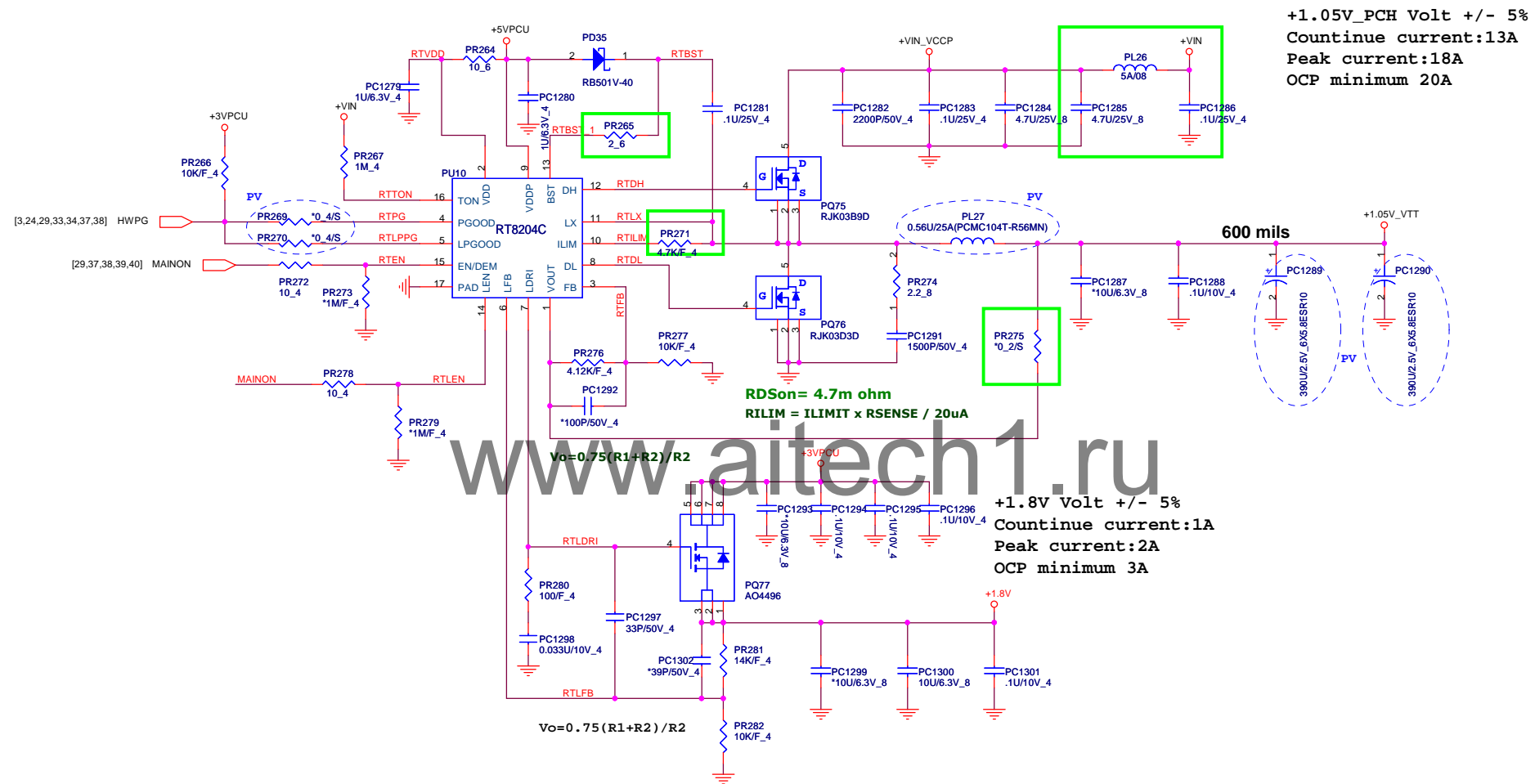


HDMI PORT







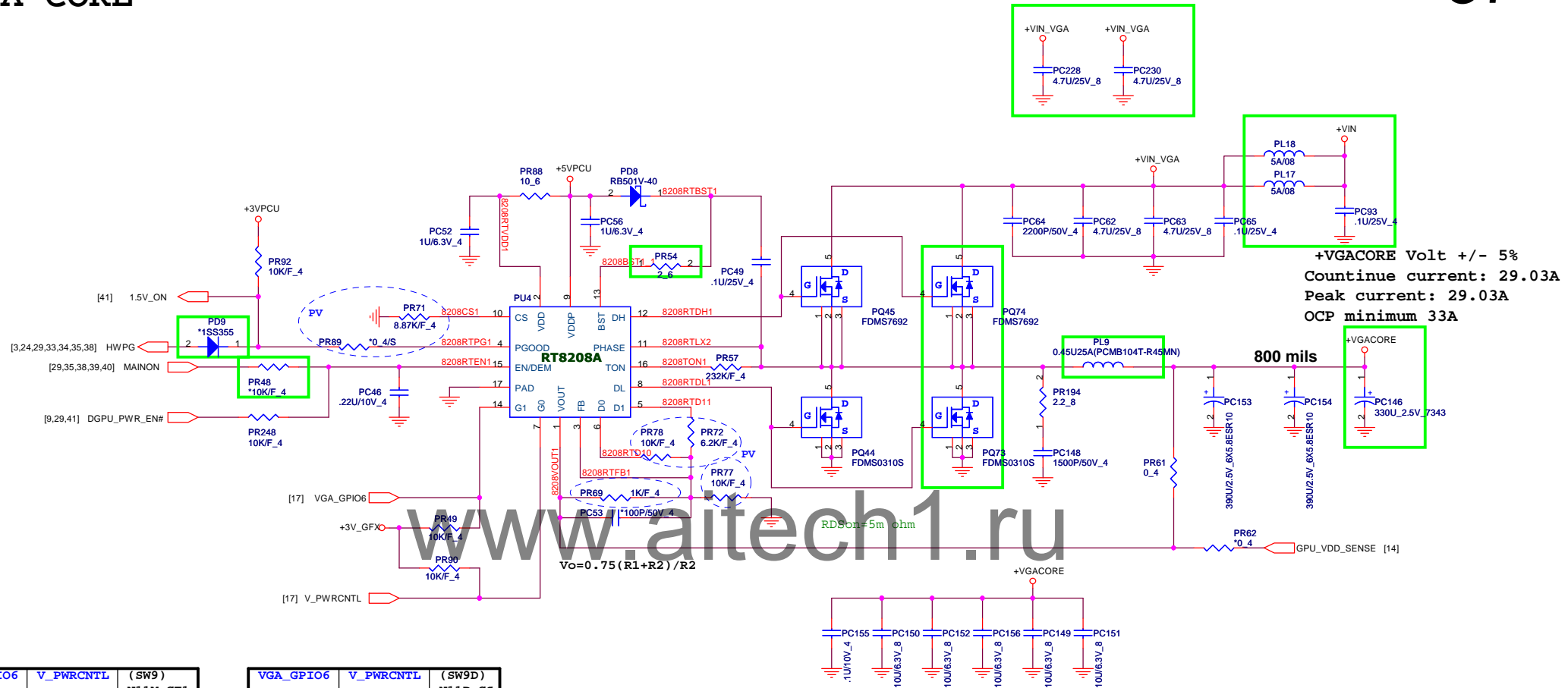


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Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH +1.05V (RT8204)	1A
Date: Friday, June 04, 2010	Sheet 35 of 43	



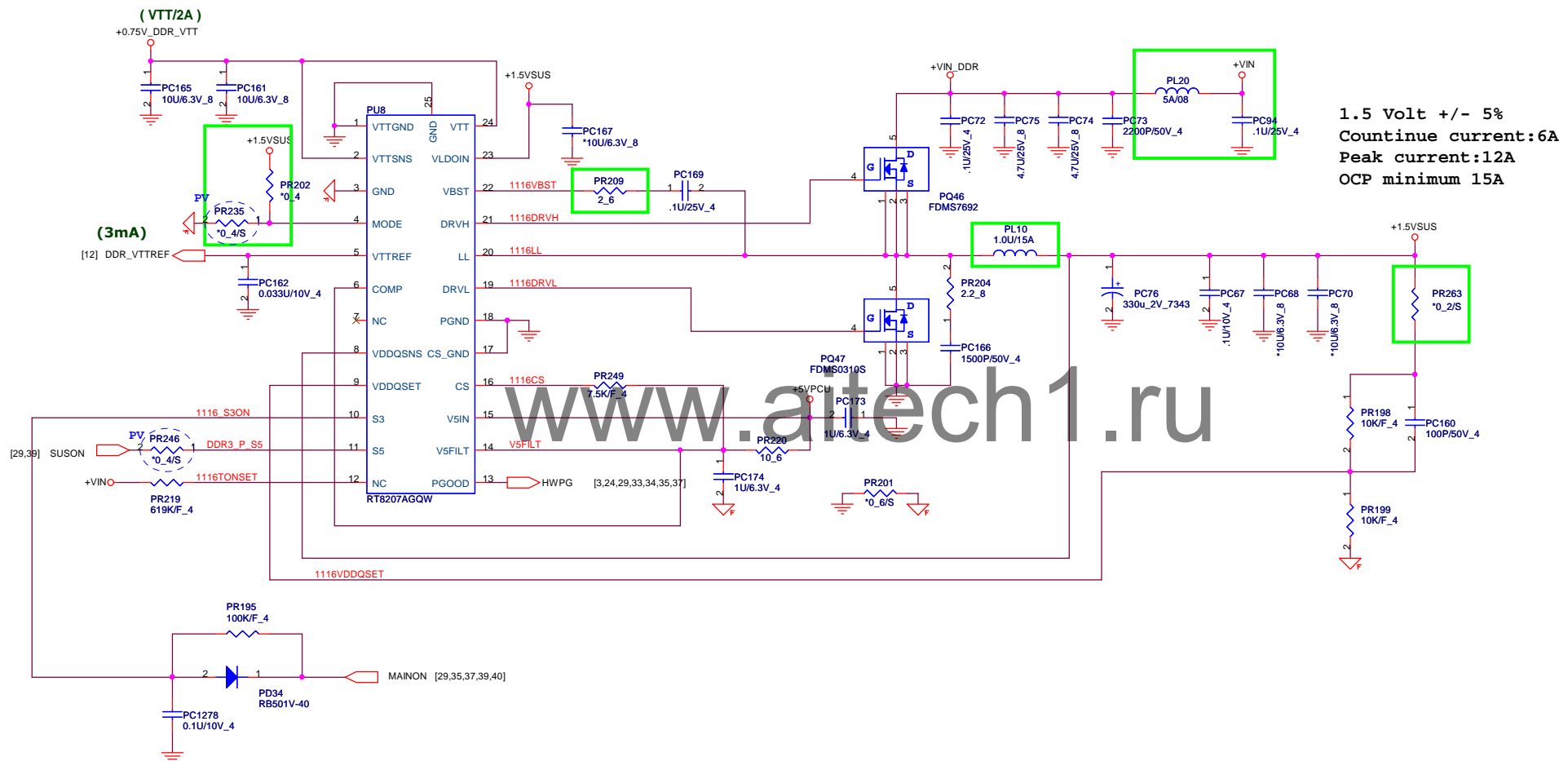
OCP Setting	Operation Max current	PR30	PR42
45W CPU (60A)	50A	1.91 Kohm	4.02 Kohm
35W CPU (48A)	40A	1.54 Kohm	4.99 Kohm

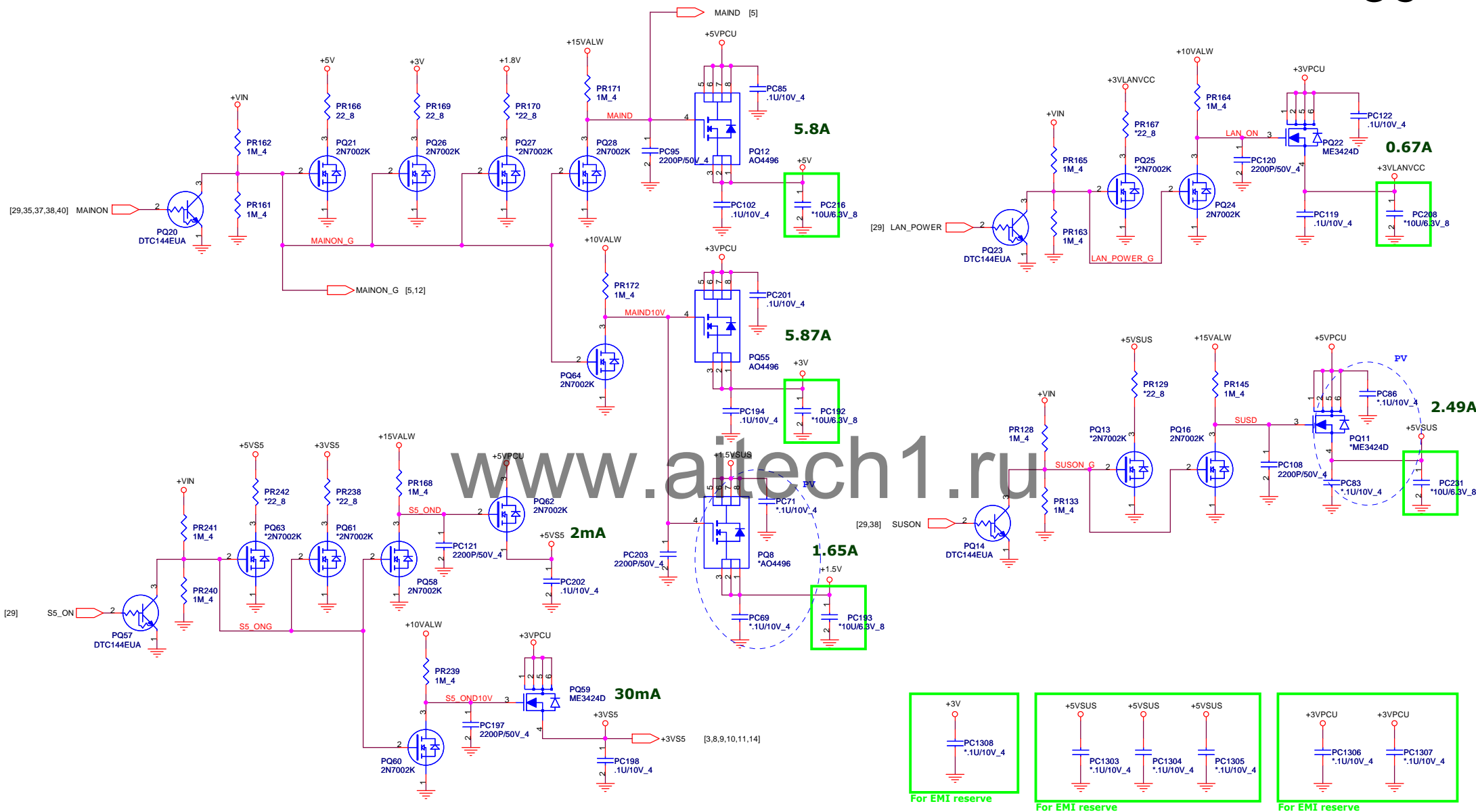


VGA_GPIO6	V_PWRCNTL	(SW9) N11M-GE1
GPIO6	GPIO5	
0	0	0.8V
0	1	0.85V
1	0	1.0V
1	1	NA

VGA_GPIO6	V_PWRCNTL	(SW9D) N11P-GS
G1	G0	
0	0	0.825V
0	1	0.9V
1	0	0.95V
1	1	1.025V

1 : un-Mount PD9/PR48 for Switchable
2 : un-Mount PR248 for Discrete

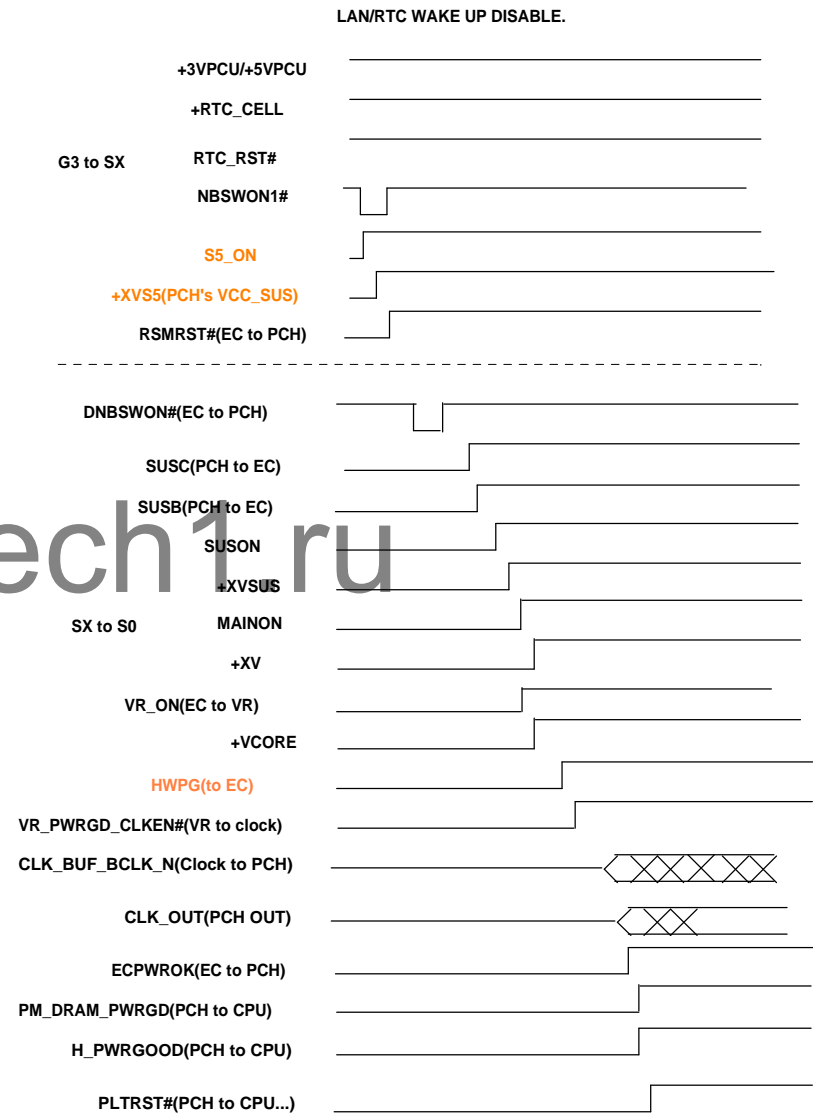
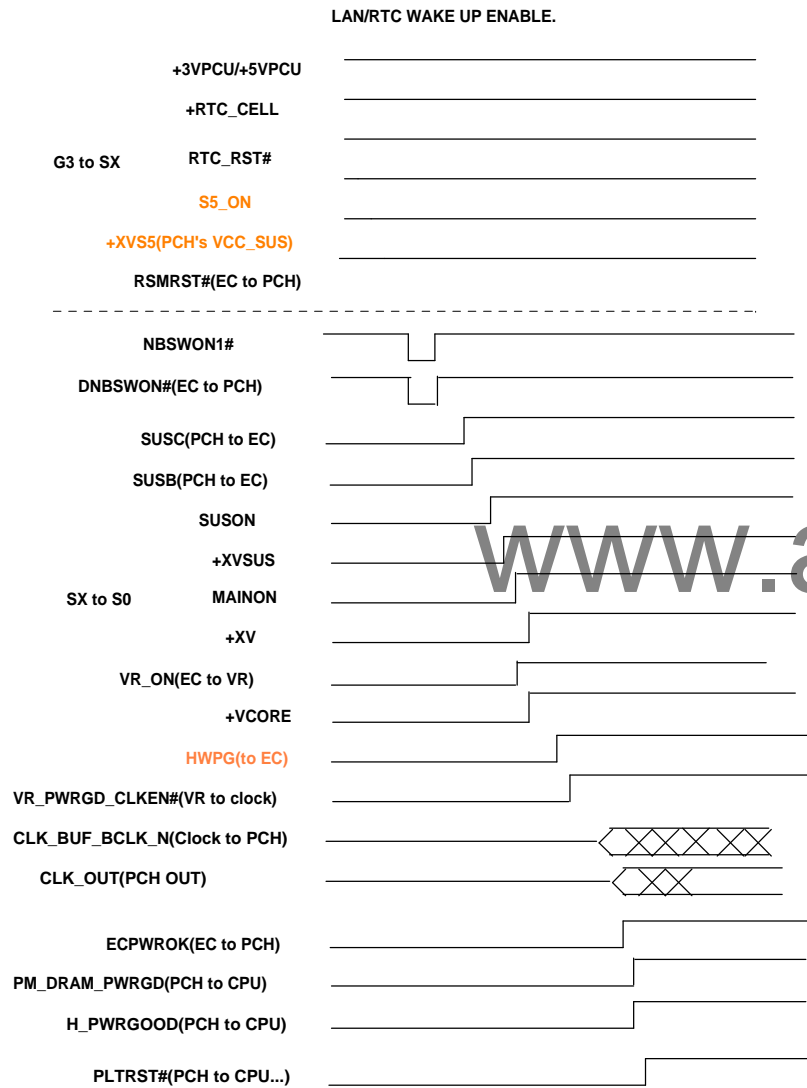






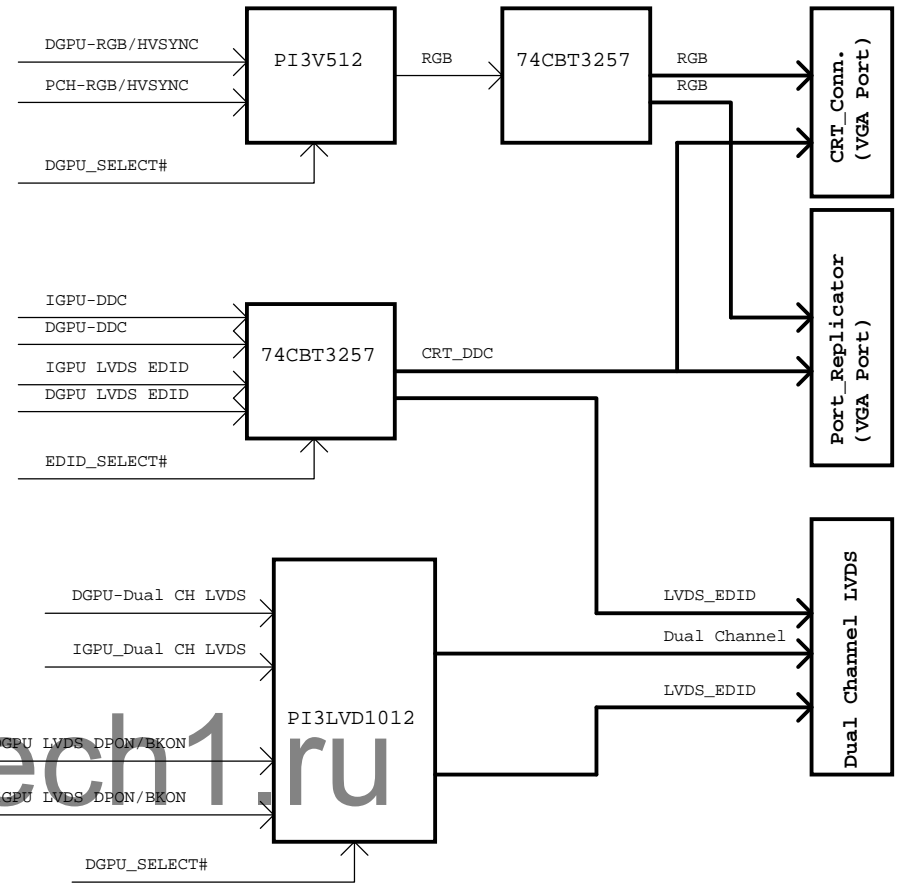
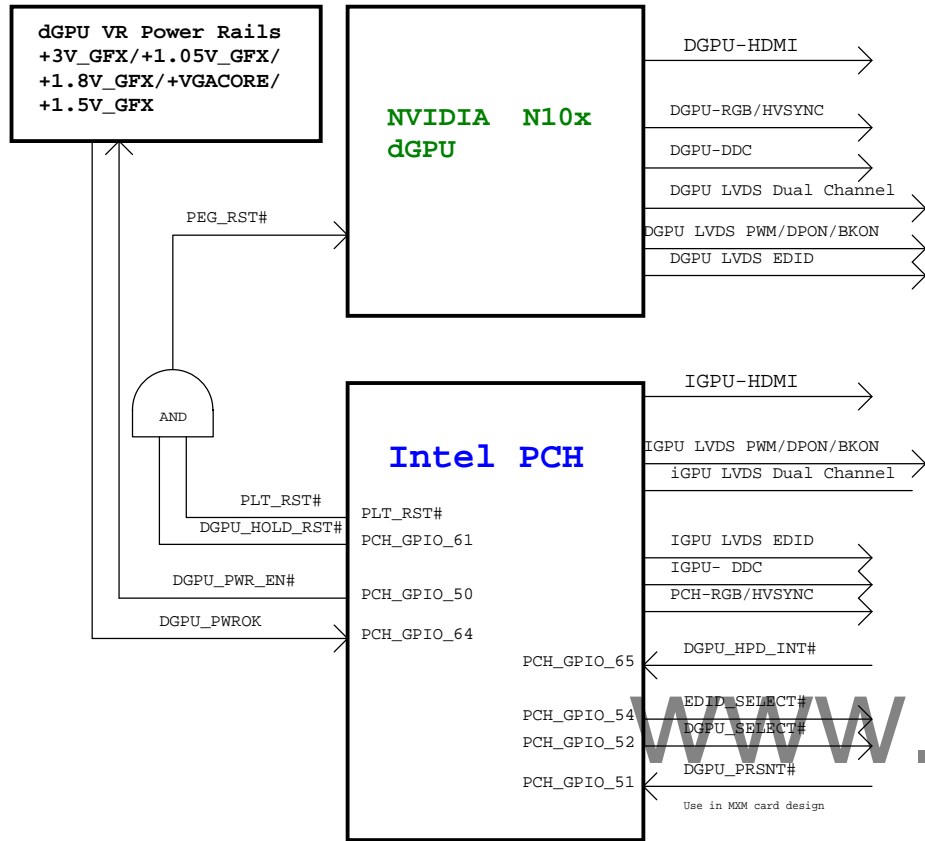
Size Custom	Document Number Charger (ISL6251)	Rev 1A
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Power up sequence



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Quanta Computer Inc.

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Switchable GPIOs	Descriptions
PCH_GPIO52	DGPU_SELECT#
PCH_GPIO61	DGPU_HOLD_RST#
PCH_GPIO50	DGPU_PWR_EN#
PCH_GPIO64	DGPU_PWR_OK
PCH_GPIO54	EDID_ELECT#
PCH_GPIO51	DGPU_PRSENT#
PCH_GPIO53	PWM_SELECT#

